

SECTION L, PART 0

REGISTER, SENDER TESTING - TROUBLE ANALYSIS

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L0 REGISTER, SENDER TESTING - TROUBLE ANALYSIS

The L section covers testing registers and senders using the Master Test Control (MTC) Circuit and Automatic Monitor Register Sender Test Circuit (AMRST). Primary control of these tests is in the MTC. The digits to be dialed are set on the keys or switches in that circuit. The tests to be made on the registers and senders are under control of the keys in the AMRST which are preoperated. The pulsing performance and other tests of the registers and senders are made and checked by the AMRST and if completed satisfactorily an OK signal is indicated.

Part L0 of the SCD describes the use of the test analysis sequence charts, test setup tables and SFD sequence charts.

L0-1 TEST SETUP TABLES

The test setup tables shown on SFD-L002, 4, and 6 summarize, in tabular form, the keys and switches used to establish a particular class of test. A single line is used to separate a particular function with its associated figure, option, key, or switch. The double line within the single lines is used to separate the various options on vintages of master test control frames. The note column and sheet notes are as follows:

- (a) Note 1 indicates that all key(s) or switch(es) must be operated to make a proper test frame setup for the particular class of test. It is suggested that known working equipment must be selected for test.
- (b) Note 2 indicates the key(s) or switch(es) to be used to simulate the trouble record.
- (c) Note 3 indicates those key(s) or switch(es) used for additional tests but they are not necessarily required for trouble record test or simulation test.
- (d) Note 4 indicates the key(s) or switch(es) located on the Automatic Monitor Register Sender Test panel.

L0-1.1 ORIGINATING REGISTER (OR) TEST (SFD-L002)

Tests of originating registers are usually made by using the Originating Test Line (OTL) as the calling line. On this type of test, the master test control circuit extends the OTL to the AMRST where subscriber line and dialing conditions are simulated. The test connection is set up by the marker under control of the master test control circuit. The

circuit. The keys or switches of the master test control circuit are operated to select the marker to establish the test connection, to set up the called number to be sent to the register, to set up the class of service of the calling line, to select the trunk link frame location of the desired register, and to select the desired register.

The keys of the AMRST are operated to prepare the circuit for a test, to set up the speed of pulsing, and to establish the calling subscriber line condition which matches the class of service set up on the master test control circuit.

When the connection to the OR has been established the AMRST outputpulses the digits set on the MTC keys or switches into the OR. When pulsing is complete the OR seizes a Completing Marker (CM). The digits stored in the OR are then passed to the CM and the AMRST. The monitor compares these digits to those it outputpulsed, if they match an OK lamp lights, if they do not match the TBL lamp lights and a trouble recorder card is perforated.

LO-1.2 SENDER (SDR) TEST (SFD-L004)

Tests of outgoing senders, without AMA, are usually made using the OTL as the calling line location. On this type of test the MTC circuit extends the OTL to the AMRST to simulate calling customer dialing. The test connection is set up by the CM, under control of the MTC. The keys of the MTC are operated to select the CM used on this test, to set up the called number to be outputpulsed by the OS, to set up the class of service of the calling line, to select the sender to be tested, and to select the outgoing trunk, if a trunk is required. A particular outgoing trunk may be used for the test by selecting a trunk that has access to the desired sender, and by operating the proper trunk selection keys.

The keys of the AMRST are operated to prepare the circuit for test, to select the sender group, and to establish certain test conditions to be applied to the sender as simulated trunk and trunk conductor conditions.

When the AMRST is ready for test, the MTC connects to the Master Test Frame Connector (MTFC) which seizes the selected marker. The MTC simulates an OR which has received a dialed number from a calling customer. The marker, having received the required information, determines the route, selects the desired sender, and selects an outgoing trunk that has access to that particular sender. The marker then establishes a connection from the Trunk Link (TL) frame location of the trunk to the Line Link (LL) frame location of the OTL. The CM selects and seizes

the desired OS through the Outsender Connector (OSC) and Outsender Link (OSL) circuits and connects the sender to the outgoing trunk. The marker then passes the called number, along with class signals and other information, to the sender. The marker makes its usual checks and releases, leaving the connection held operated under control of the test circuit. With this connection, the test circuit simulates the calling customer and incoming trunk in the distant office. The sender makes the required test of trunk conductors and trunk conditions and then starts to pulse out the called number. The outgoing end of the trunk is connected to the AMRST. The AMRST receives and records the pulses from the OS via the M relay. The AMRST then matches the called number received from the sender against the called number received from the MTC circuit. If they match, an OK lamp lights on the monitor panel; if they do not match, the TBL lamp lights and a trouble recorder card is perforated.

L0-1.3 INCOMING REGISTER (IR) TEST (SFD-L006)

On an Incoming Register (IR) class of test, the MTC is used only to provide the called number and certain incoming class information which the IR normally receives from the Incoming Register Link (IRL) circuit. The IR group key(s) or switch(es) of the AMRST are operated to prepare the MTC for selection of the incoming register group and IR to be tested. Also, various key(s) for test conditions of IR and IRL, and selected speed of pulsing are operated.

The MTC seizes the desired IR through the special test appearance at the IRL. In each IRL group, the "0" vertical of horizontal group 0 is reserved for the AMRST appearance. The test vertical appears in the IRL group in the same manner as an incoming trunk. The AMRST calls for the desired IR through the trunk preference chain in the IRL group as an incoming trunk does. When the AMRST has seized the IR, it makes preliminary tests and then pulses the called number into the IR.

After the number is pulsed and recorded in the IR, it seizes its associated IRMC and selected marker. The called number is then passed to the CM and AMRST circuit through the MTFC. The AMRST matches the called number passed to it from the IR with the number pulsed into the IR. If they match, the OK lamp lights on test panel. Failure to match results in the TBL lamp lighting and a trouble record card is perforated.

On this type of test, the marker does not establish any connections to LL or TL frames.

L0-2 TEST ANALYSIS SEQUENCE CHARTS (SFD-L003,5,7)

Test analysis sequence charts depict lamp sequence at the MTF, as opposed to standard sequence charts which show a sequence of relay operations and releases. These test analysis sequence charts are intended as additional trouble shooting aids.

L0-2.1 USE OF TEST ANALYSIS SEQUENCE CHARTS

These paragraphs will demonstrate the use of the Test Analysis Sequence Charts (SFD-L003,5,7). The test analysis sequence charts, and all sequence charts, operate from top to bottom. To identify the trouble area the user, reading from top to bottom, compares the lamp indications at the MTF with that trouble analysis sequence chart to determine at what point the progress stopped.

To demonstrate (SFD-L003): Working down the test analysis sequence chart, all lamps are indicated down to the CKS lamp which did not light. The problem exists between the MST and CKS lamps. The sheet coordinate L302/-- within the double line box, refers to the sequence chart where the detail of the operation can be found. Use of this sequence chart will be described in L0-3.

L0-3 SEQUENCE CHARTS

The sequence charts used in the SFD follow standard conventions for sequence charts, except as noted on SFD-A103. However, the sequence charts in the L section depict the switch type MTC circuit with connector SD-27719-01.

The example in L0-2.1 continues on SFD-L302. The CKS lamp checks that the CKS relay operates. The CKS relay checks that the RTC2, LT, PK, ORT, DPT, or MFT relays have operated and that the CL and TRNA switches are operated. If the CKS relay in fact has not operated it is necessary to check if all relays in its path have operated. If they have all operated, the user should now check the CKS operate path. If one or more of these relays have not operated the same procedure should be taken for these relays as taken for the CKS.

SECTION L, PART 1

REGISTER AND SENDER TESTING - ESTABLISHING THE CONNECTION

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L REGISTER AND SENDER TESTING

The general sequence of operation of register and sender testing is as follows:

(a) Originating Register Testing

Primary control of this test is in the Master Test Control (MTC) circuit. The tests to be made on the Originating Register (OR) are under control of the keys in the Automatic Monitor Register Sender Test (AMRST) circuit which are pre-operated. The digits to be outputted by the AMRST the OR, as set in the MTC, are registered in the AMRST. A direct connection between the OR and the AMRST is established via the M relay in the OR for control purposes. The MTC, via the Master Test Frame Connector (MTFC), selects a marker which connects the Originating Test Line (OTL) to the desired register as for a dial tone connection. The line end of the OTL is connected through the MTC to the AMRST where it connects to a loop closure controlled by the Dial Pulse or TOUCH-TONE signal generator, simulating a subscriber.

With the MTC circuit connected to the OR via the OTL the AMRST pulses the digits set on the keys or switches of the MTC into the OR where they are recorded and stored.

When the OR recognizes that pulsing is completed, it seizes a Completing Marker (CM) through the originating register marker connector ORMC. The marker, recognizing it is handling a monitor test call, (MON relay operated), stops its regular progress and seizes the MTFC which connects to the AMRST. The digits stored in the OR, along with other information, are passed through the ORMC, CM, and MTFC to the AMRST where they are checked against the digits that were pulsed into the OR. If the digits match the test has been completed satisfactorily and an OK signal is indicated. This starts release of the OR. Operation of the RL key in the MTC starts the release of the AMRST, however the AMRST and the OR will not fully release until the STT key in the AMRST has been released.

(b) Sender Testing

In this test the MTC selects a CM and causes the marker to select the desired sender and prime it as directed by the MTC. The called number and class information, as set on the keys and switches in the MTC, is transmitted and stored in the Outgoing Sender (OS) and AMRST. A direct connection between the OS and the AMRST is established via the M relay in the AMRST for pulse receiving by the AMRST. The OS is connected to an Outgoing Trunk (OGT) and the originating end of the OGT is connected to the OTL. The TT relay is operated in the OGT

to disconnect the completing tip and ring from the distant office and connect them to the AMRST to control supervision. The AMRST then has control of both ends of the trunk.

After the OS receives the start pulse signal from the AMRST the digits stored in the OS are outputted into the AMRST via the OS M relay where they are recorded and stored.

After the sender completes outputting, the digits outputted by the sender into the monitor are checked against the digits that were stored in the monitor at the start of the test by the MTC. If the digits match, the test has been completed satisfactorily and an OK signal is indicated. This starts release of the sender. Operation of the RL key in the MTC starts release of the AMRST, however, the AMRST and OS will not fully release until the STT key in the AMRST has been released.

(c) Incoming Register Testing

On an Incoming Register (IR) IR test the MTC connects to the AMRST which selects the register to be tested. The digits to be outputted by the AMRST into the IR, as set in the MTC, are registered and stored in the AMRST. The AMRST sets up a connection to the IR through its appearance on the Incoming Register Link (IRL) frame (TPOO). A direct connection between the IR and AMRST is established via the M relay in the IR for control purposes. After the AMRST and the IR are connected via the IRL, seven prepulsing tests are made upon the IR by the AMRST.

After these IR tests have been completed satisfactorily the AMRST pulses the digits set on the keys or switches of the MTC into the OR where they are recorded and stored.

When the IR recognizes pulsing is completed, it seizes a CM through the Incoming Register Marker Connector (IRMC). The marker, recognizing it is handling a monitor test call (MON relay operated), stops its regular progress and seizes the MTFC which connects to the AMRST. The digits stored in the IR, along with other information, are passed through the IRMC, CM, and MTFC to the AMRST where they are checked against the digits that were outputted into the IR. If the digits match the test has been completed satisfactorily and an OK signal is indicated. This starts release of the register. Operation of the RL key in the MTC starts the release of the AMRST, however, the AMRST and the IR will not fully release until the STT key in the AMRST has been released.

L1 ESTABLISHING THE CONNECTION

Part L1 describes how the AMRST establishes a connection to the register or sender to be tested. This description is separated by test type.

L1-1 ORIGINATING REGISTER TESTING

Primary control of this test is in the MTC circuit. The tests to be made on the OR are under control of the keys in the AMRST which are preoperated. The digits to be outputted by the AMRST into the OR, as set in the MTC, are registered in the AMRST. A direct connection between the register and the AMRST is established via the M relay in the OR for control purposes. The MTC, via the MTFC, selects a CM which connects the OTL to the desired OR as for a dial tone connection. The line end of the OTL is connected through the MTC to the AMRST where it connects to a loop closure controlled by the dial pulse or TOUCH-TONE signal generator, simulating a subscriber. The AMRST can now test the register via the OTL.

L1-1.1 MONITOR PREPARATION (SFD-L105)

Before the AMRST is connected to the OR to be tested, it is necessary to prepare the AMRST for testing. At the MTC the OR key is operated or TSTA switch is set to the OR position, followed by operation of the STT key. This operates the STT relay from ground over lead STT from the MTC. The STT served as a general off-normal relay for the testing operation of the AMRST. The digits to be pulsed are set up on the digit keys or switches in the MTC. The particular tests and pulsing conditions are set up on keys and switches as described in the paragraphs which follow. The pulsing conditions must be set prior to starting the test.

L1-1.1.1 Type of Register (SFD-L105)

If TOUCH-TONE tests are to be made on the OR, the PB key should also be operated which operates the POR1 relay. For dial pulse tests the PB key is left normal.

With the PB key normal, STT operates the DOR1 relay. With PB key operated, STT operates POR1 which, in turn, operates DOR1. Relay DOR1 operates the ORD relay, when POR1 is normal, to prepare the dial pulse generator for OR testing, or the ORP relay, when POR1 is operated, to start the TOUCH-TONE signal oscillators and prepare the TOUCH-TONE

signal generator for OR testing (SFD-L106). Relay DOR1 operates DOR3 to prepare the originating register test controller for testing. Relay DOR1 also supplies battery through the NTC resistance to the N lead to the MTC circuit to make effective the SRT1 relay of that circuit. The OR key or TSTA switch to OR position of the MTC and the DOR1, POR1, ORD, and ORP relays of the AMRST will remain operated during OR testing and are not released between test calls.

L1-1.2 START OF TEST (SFD-L107)

After the ST key, SRT1, N and N1 relays have operated in the MTC the DOR2 relay operates from ground on the STG lead. Relay DOR2 operates ONT1 and ONT2 relays which serve as cut-in relays and also furnish general testing off-normal grounds. Relay ONT1 starts the TM timer, which provides each test call with a single 40 to 70 second time interval, by operating relays TMA and TMB, and operates the TSR relay. Relay ONT1 closes a ground to the PCO lead to the traffic register circuit to operate a register which indicates the number of originating register test calls (SFD-L326). The DOR2 relay serves as a cut-in relay for leads from the OR to the AMRST. The DOR2 operates ORST which furnishes off-normal grounds to prepare for the originating register tests, the dial pulse or TOUCH-TONE signal generators, and the outpulsing steerer for an originating register test call.

L1-1.2.1 MTC Control

The operation of the ST key also causes the MTC circuit to connect to a CM through the MTFC causes that CM to establish a connection between the OTL and the OR to be tested. The line end of the OTL is at the same time connected through the MTC circuit to the STT relay. The tip and ring are extended through the operated STT and DOR2 relays and the unoperated CN and 2P relays and the unoperated POR2 relay to the dial pulse generator or the operated POR2 relay to the TOUCH-TONE generator where a loop closure is provided under control of either the dial pulse or the TOUCH-TONE signal generator (SFD-L224).

L1-1.3 REGISTER CONTROL - OPERATION OF M RELAY (SFD-L109)

The MTC circuit supplies a ground which, through the CM and the trunk link frame and connector circuit (TCL), operates the M relay of the OR. The M relay locks to the DOR2 relay and closes signaling leads from the OR to the AMRST. Ground on the MST lead from the OR operates the RPS2 relay. Relay RPS2 closes an operating ground for RPE2, but that relay does not operate at this time due to a shunting ground on the MST lead.

L1-2 SENDER TESTING

In this test the MTC Circuit selects a CM and causes the marker to select the desired OS and prime it as directed by the MTC. The called number and class information as set on the keys and switches in the MTC, is transmitted and stored in the OS and AMRST. A direct connection between the OS and the AMRST is established via the M relay in the OS for pulse receiving by the AMRST. The OS is connected to an Outgoing Trunk (OGT) and the originating end of the OGT is connected to the OTL. The TT relay is operated in the OGT to disconnect the completing tip and ring from the distant office and connect them to the AMRST to control supervision. The AMRST then has control of both ends of the trunk.

L1-2.1 MONITOR PREPARATION FOR SENDER TEST (SFD-L105)

Before the AMRST is connected to the OS to be tested, it is necessary to prepare the AMRST for testing. The SDR key is operated or TSTA switch is set to the SDR position at the master test control, followed by operation of the STT key. This operates the STT relay from ground over lead STT from the master test control circuit. The STT serves as a general off-normal relay for the testing operation of the AMRST. The MAC key should be operated and the tubes of the amplifier be permitted to heat for one minute before a sender is selected. The tests to be applied to the sender are selected by keys as described in subsequent paragraphs.

L1-2.1.1 Type of Sender (SFD-L105)

The SGT key is operated, or the SG SEL switch is set at the position associated with the outsender group in which the sender to be tested is located, or the SG- key, associated with the outsender group in which the sender to be tested is located, is operated. Ground from STT through the SGT key, or the SG SEL switch, or the SG- key, operates the DOS1 or MOS1 relay depending on whether the sender group is dial or multifrequency pulsing. The DOS1 relay operates the AON relay and the DPST relay. These three relays prepare the AMRST for testing dial pulse senders. Relay MOS1 operates MFST to prepare for testing multifrequency senders. Relay DOS1 or MOS1 supplies battery through the NTC resistor to the N lead to the master test control circuit to make effective the SRT1 relay of that circuit. All the foregoing relays remain operated between calls.

L1-2.2 START OF SDR TEST (SFD-L107)

After the ST key, SRT1, N and N1 relays have operated in the MTC, the DOS2 or MOS2 relay operates to ground on the STG lead. Relay DOS2 or MOS2 operates ONT1 and ONT2 which serve as cut-in relays and also furnish general testing off-normal grounds. Relay ONT1 starts the TM timer, which provides each test call with a single 40 to 70 second time interval, by a ground operating relays TMA and TMB, and operates the TSR relay.

Relay ONT1 closes a ground to the PCS(DP) or PCS(MF) lead to the traffic register circuit to operate a register which indicates, respectively, the number of dial pulse or multifrequency sender test calls (SFD-L326). Relay ONT2 operates ONR to furnish off-normal grounds. Relay MOS2 or DOS2 operates ONS which serves as an off-normal relay which releases between calls. Relay MOS2 operates MFS and in turn MFN to prepare the multifrequency amplifier and associated receiver for receiving multifrequency pulses. Similarly, DOS2 operates DON to prepare for counting the dial pulses.

L1-2.2.1 MTC Control

The ST key of the MTC circuit also causes that circuit to seize a marker through the master test frame connector. The CM is primed by the MTC circuit and proceeds to set up a connection from the originating test line to a trunk and from the trunk to the particular sender selected for test. The CM causes the TT test relay in the outgoing trunk to operate and connects the outgoing tip and ring of the trunk to the AMRST.

L1-2.2.2 Connection of Monitor to Marker and Sender

As the MTC circuit connects to the MTFC, it grounds the MC lead to the AMRST, operating the CII relay through MOS1 or DOS1 (SFD-L115). Relay CII operates the MCA, MCB (SFD-L309), MCI, and MCJ relays to connect the AMRST to the MTC circuit since that circuit already has control of the MTFC preference chain and control circuit. The cut-in relays at the marker end of the MTFC are operated by the MTC circuit.

The MT relay is connected through the DOS1 or MOS1 relay and the MCA relay to the MON lead to the MTFC (SFD-L318). When the connection is completed to the CM, the CM MT relay operates in series with the MON relay of the marker. The MON relay locks to MT on the direct MONL lead from CM to AMRST. The MON relay of the marker prepares the marker for operation with the AMRST, serving principally as a cut-in relay for direct leads from AMRST to CM. Relay MON also operates MON1 of the CM.

When the CM selects the OS through the OSC, the M relay of the OS operates from ground supplied from MOS1 or DOS1 through a break contact of SON1 on the OSM lead to the CM and through the OSC to the M relay (SFD-L115). The M relay locks to ground on the LK lead supplied by MOS2 or DOS2. A holding ground for the SB relay of the OS is furnished by MOS2 or DOS2 on the SB lead to the sender. Relay DOS2 or MOS2 and the sender M relay serve as cut-in relays for leads from OS to AMRST.

Ground from the STT relay to the SG lead to the OS is returned through the sender M relay on the MOS or DOS lead and through MOS2 or DOS2 to operate SON1.

Relay SON1 operates MCC through C11. Relay SON1 opens the OSM lead to the CM and closes the RA lead from the marker to the MTR relay. Both of these latter functions were provided to care for route advance of the marker after it had selected an OS. With the marker under control of the MTC circuit during testing, route advance will not be used and these functions of the SON1 relay are not used.

L1-2.2.3 Digit Registration - Input to Sender (SFD-L120)

The called number is registered on the KA-L(2/5) relays in the AMRST. The KA-L relays operate through the MCB relay. The called number is the number passed from the keys or switches of the MTC circuit to the CM and through the marker to the OS. However, the CM may instruct the OS to modify this number before it is outputted. The AMRST registers such information passed from CM to OS on leads carried through the MCI and MCJ relays (SFD-L117). If the CL1 relay operates, it indicates that either a one-one prefix or a fixed XX prefix is to be outputted by the OS on a CL1 class basis. The wiring options for this feature must be coordinated with the wiring arrangement in the senders. The CL(2-6) relays and CL(7-8) relays register further class information for trouble record and test purposes. If any digits are not to be outputted, one of the DL(1-7) relays will operate. The DL1 relay is associated with the A digit and the DL2 relay with the B digit, etc. If a DL- relay is operated, its associated digit and the preceding digits up to and including the A digit will be deleted.

The information described above is passed from CM to OS through a connector common to a number of senders and for this reason is held by the marker only for a timed interval long enough to register and check the information passed to the OS. In order to be sure that the AMRST obtains this information, the MON relay of the marker stops the marker timing of the OSC holding interval. When a path has been established for registering this information, a ground through the marker cut-in relays of the MTFC will be connected to the SCT lead to the AMRST and through the MCI and MCJ relays to the SCT lead to the marker where it operates the SCT relay (SFD-L309). The SCT relay permits the marker SCT timing to continue. The CM timing being sufficient to permit the AMRST to register this information.

L1-2.2.4 Line Link Identification (SFD-L118)

The location of the originating test line will be recorded through the MCA relay. The number of the CM handling the call is recorded through the MCA relay. Ground is connected to one of the DRA(0-9) leads through the operated MTFC cut-in relay of the marker. This ground operates an M(0-9) relay for the marker units number. If there are more than 10 markers, one of the relays MKT0 or MKT1 will be operated to indicate the tens number (SFD-L310).

L1-2.2.5 Trunk Link Identification (SFD-L115,16)

The location of the outgoing trunk on the trunk link frame is carried through the MCC relay. A battery, connected through the MCC relay to the TRA lead to the MTFC and then to the Trunk Link Frame (TLF) through the marker cut-in relays, causes operation of relays which furnish trunk location information to the AMRST. The switch on which the trunk appears is registered on the LC(0-9) relays on a 1-out-of-10 basis. The level on the switch is registered on the LV(0-9) relays on a 1-out-of-10 basis. The FAK and FBK relays register whether the trunk is an A or B appearance on the switch level. The FS(0-29) relays operate directly from the marker and indicates the trunk link frame number on a 1-out-of-30 basis.

The trunk location information relays of the AMRST are not locked up until the marker grounds the HMS1 lead to the AMRST (SFD-L115). This indicates that the marker has reached the point of operating the channel hold magnets. This delay in locking the relays is provided to permit the marker to change trunks prior to grounding the HMS1 lead. The HMS1 ground through MCA operates TLG. Relay TLG locks and operates LVG, LCG, FSG1, and FSG2. These relays furnish locking grounds for the trunk identification relays. Individual locking grounds are supplied for these relays. This prevents backups through the locking contacts of these relays as the trunk location information changes. When all the ground supply relays have operated, RTC1 is operated.

L1-2.2.6 Release of Master Test Frame Connector (SFD-L115)

After RTC1 operates, it locks, opens the MON1 lead to the CM, and operates RTC2. Relay RTC2 releases marker MON1 relay (SFD-L309). Relay RTC2 releases C11 and in turn MCA, MCB, MCC, MCI, and MCJ to disconnect the AMRST from the MTFC. Relay RTC2 connects ground through DOS1 or MOS1 to prime the steering circuit. This action is delayed until this time because the information received from the marker will determine which steering relay is to be operated.

L1-2.3 INTERMARKER GROUP SENDER TEST

Intermarker Group Senders (IMS) perform the functions of an OS in the calling marker group and those of an IR in the called marker group. With this arrangement no outpulsing is required and the called number is passed through the sender from the calling marker group to the called marker group.

The keys on the MTC circuit are operated to select the intermarker group sender to be tested, the marker to be used, and to set up the called number, the calling line location, and the calling line class of service. Unlike the outgoing sender tests, the intermarker group sender tests use the AMRST or the sender test set with the telephone circuit only for observing certain tone indications.

When the circuits are ready for test, the MTC circuit signals the CM that this is a test call. The marker, having received the necessary information, determines the route and selects the intermarker group trunk. It sets up a connection from the TLF location of the selected intermarker group trunk to the line link frame location of the originating test line. The marker selects and seizes the desired IMS through connections on the sender link and connects the sender to the trunk. The called number is then passed from the marker to the IMS where it is stored. The test signal is also sent to the sender, operating a test relay.

If the REC key on the MTC is operated, causing the calling marker to take a trouble recorder card of the established connection. The marker is then released and the connection is held under control of the MTC circuit.

The IMS, having received the called number, connects to an incoming register marker connector in the called marker group. The connector selects a marker in that group and passes the called number and a test signal to the called marker. When the called marker receives the test signal, it blocks and takes a trouble recorder card which shows also a sender test indication. If the called number and IMS number on both cards correspond with the information set up on the MTC circuit keys, the test is satisfactory. After the trouble recorder cards are taken, the marker releases and the connection is held under control of the MTC circuit.

L1-3 INCOMING REGISTER TESTING

On an IR test the MTC connects to the AMRST which selects the IR to be tested. The digits to be outpulsed by the AMRST into the IR, as set in the MTC, are registered and stored in the monitor. The monitor sets up a connection to the register through its appearance on the IRL frame (TP00). A direct connection between the IR- and AMRST is established via the M relay in the IR for control purposes. After the AMRST and the IR are connected via the IRL certain tests are made upon the register by the AMRST.

L1-3.1 AMRST PREPARATION FOR IR TEST (SFD-L105)

Before the AMRST is connected to the IR to be tested, it is necessary to prepare the AMRST for testing. The IR key is operated or TSTA switch is set to IR position at the MTC, followed by operation of the STT key. This operates the STT relay from ground over lead STT from the MTC circuit. The STT serves as a general off-normal relay for the testing operation of the AMRST. The digits to be pulsed are set up on the digit keys or switches in the MTC. The particular tests and pulsing conditions are set up on keys and switches as described in the paragraphs which follow.

L1-3.1.1 Type of Incoming Register (SFD-L105)

The number of the incoming register group is set up on the IG- keys or IRG switch in the AMRST. The key or switch is operated to the position corresponding to the number of the incoming group in which the IR to be tested is located. The number of the IR within its group is selected by setting the corresponding number on the SRS key or switch (SFD-L108). Ground from the STT relay through the IG- key or IRG switch operates the DIR1 or MIR1 relay depending on whether the register group is dial pulse or multifrequency. Either of these relays operate all of the SPR-relays (SFD-L108). The SPR- relays open the paths by which the IRP- (SFD-P113) relays are operated from the IRL's. The PC- relay operates through the SPR- relay and the selected incoming register group key or switch. The PC- relay connects the windings of the ten IRP- relays of its incoming register group to the 0-9 settings on the SRS key or switch.

If MIR1 operates, it operates MR, and MF to prepare those circuits for multifrequency operation. If DIR1 operates, it operates IRD and in turn DP to establish dial incoming register test conditions in that circuit. Relay DIR1 also operates DR which prepares the incoming register test controller for dial register testing. Relay DR or MR supplies ground which operates bylink relay BL or nonbylink relay NBL depending upon the position of the BL key. Either the DR or MR relay supplies ground to operate the NDT relay. All of the relays discussed thus far remain operated as long as the associated keys remain operated and do not release between calls. However, release of the STT key will release all operated relays.

Either DIR1 or MIR1 operates BT1 (SFD-L208) which supplies battery through the NTC resistance to the N lead to the MTC circuit to make the SRT1 relay of that circuit effective.

L1-3.2 START OF TEST (SFD-L107)

After the ST key, SRT1, N and N1 relays have operated in the MTC the BT2 relay operates to ground on the STG lead. Relay BT2 operates the IRP-relay associated with the register selected by connecting operating battery and ground for the IRP relays (SFD-L108). Relay BT2 operates STK to supply off-normal grounds. Relay BT2 also opens the operating path of BT1.

When IRP- operates, it operates the M relay of the IR which connects leads from IR to AMRST which are used for control purposes. A ground from IRP- is connected to the MB lead to the IR to operate MB of the register. Relay MB operates RB of the IR make the register busy (SFD-L110). If a call is in progress, RB will already be operated and the path just described will serve to hold the register busy at the conclusion of the call. The winding of the ON relay of the IR is connected through the M relay to the H lead to the AMRST where it connects to the winding of BT1 through make contacts of BT1. If a call is in progress, the ground which holds the ON relay will also hold the BT1 (SFD-L208). When the register becomes idle, BT1 releases and closes ground to the IRP- relay contact associated with the last register. This ground is returned through the operated IRP- relay to a testing off-normal relay. For dial registers, the DIR2 relay will operate through contacts of DIR1. For MF registers, MIR2 will operate through contacts of MIR1 (SFD-L107). Relay BT1 is slow-release to hold over the operate time of IRP- and M and also to permit the register to fully release before it is reseized.

The DIR2 or MIR2 relay serves as a cut-in relay for the leads from IR to AMRST previously closed at the register end by the M relay. Relay DIR2 or MIR2 operates ONT1 and ONT2 which serve as cut-in relays and also furnish general testing off-normal grounds. Relay ONT1 starts the TM timer which provides each test call with a single 40- to 70-second time interval by operating TMA and TMB and operates the TSR relay.

Relay ONT1 closes a ground to the PCI(DP) or PCI(MF) lead to the traffic register circuit to operate a register which indicates, respectively, the number of dial or multifrequency register test calls (SFD-L326). With the register now idle but held busy to service calls, DIR2 or MIR2 operates the IRST relay to start selection of the IR through the IRL.

L1-3.2.1 Seizure of Link (SFD-L107)

After the register has been found to be normal, the DIR2 or MIR2 operates the incoming register start relay IRST.

On bylink tests, IRST operates relay DLP (SFD-L208), which operates relay SY to advance the dial pulse generator through its interdigital timing so that it will be ready to pulse immediately when signaled to do

so. Relay IRST also supplies several off-normal grounds, one of which lights the RB progress lamp, and another that closes a circuit from battery through resistor ST, a make contact of relay IRST, break contacts of C, LKT, and BL1, a make contact of an operated PC- relay, over the ST lead through the IRL, and through the winding of test preference relay TP to ground (SFD-L110).

Operation of relay TP in the IRL locks out all trunks of horizontal group zero which have not already operated their preference relays, but the test circuit must wait until any trunks which have preference relays operated have been served. When all preference relays of horizontal group zero are normal except the test preference relay, the link grounds lead B, operating the associated trunk class relay TCL-. This relay operates the associated lock-out and operate register preference relays LO- and ORP- in the AMRST (SFD-L110).

L1-3.2.2 Register Busy (RB) Test (SFD-L110)

Relay LO operating closes a register busy lead RB0-9 from ground through the primary winding of the RB1 relay through the register link to the IR under test. Since the register has been made busy by the test circuit, the register should have battery connected to lead RB0.

The IRL has ground connected to the RB0 lead through the RB0 relay winding, but relay RB1 in the AMRST will operate with this shunt. Relay RB1 locks on its secondary winding. Resistor B is provided to prevent overheating the primary winding.

L1-3.2.3 Link Operated (LO) Test (SFD-L110)

Relay RB1 operates RB2 in the AMRST, which operates the register preference relay RP0 in the IRL by connecting ground to the RP0-9 lead. Relay RB2 also transfers the progress indication from lamp RB2 to LO and transfers the RB0 lead to the winding of relay RB3. The IRL RP relay connects the RB lead to lead LO to the register, where there should be a solid ground through the RLK normal. Relay RB3 in the AMRST tests for this ground. If this ground is missing, the RB lead will be connected in the register link and register to resistance ground and battery. Since relay RB3 is connected to resistance ground and battery, it will operate if direct ground from the IR LO lead is found, but will not operate otherwise because it will then be in a balanced bridge circuit.

When the RP relay of the IRL operates it operates the ON relay of the IR (SFD-L208). The ON operating ground operates TAC in the AMRST over the H lead from the register. Relay TAC operates TAC1 which locks to ONT1. Relay TAC1 connects a resistance ground through the TAC winding to the H lead to the register. This ground serves to hold the ON relay if its register operating ground is removed. The TAC relay is a polarized relay which will hold operated to the register ground even when

shunted by the TAC1 resistor. However, when the register attempts to release as evidenced by removal of ground from the H lead, the current through TAC will reverse, and TAC will release. If TAC releases following the operation of TAC1, TAC2 will operate. This relay arrangement thus permits holding the register off-normal for trouble tracing purposes while the same time recognizing when the release circuit of the register functions.

Ground on the MST lead from the IR through DIR2 or MIR2 operates RPS2. Relay RPS2 closes an operating ground for RPE2, but that relay does not operate at this time due to the shunting ground on the MST lead (SFD-L208).

L1-3.2.4 Lock Check (LK) Test (SFD-L110)

When relay RB3 operates, it locks, transfers the progress indication from lamp L0 to lamp LK, and connects lead LK from the IRL to the winding of relay LK. The IR should have resistance battery connected to lead LK, which will operate relay LK. This places the link connection under control of the IR by connecting the LK lead battery to lead ST.

L1-3.2.5 Operate Hold Magnet (OH) Test (SFD-L111)

Relay LK, in operating, transfers the progress indication from the LK lamp to lamp OH and connects lead OH from the link to the winding of relay OH. Relay LK also grounds lead DPG toward the register to operate the DP direct pulsing relay of the register if a dial pulse register is being tested. The register should operate its link select magnets and ground lead OH to the link. The select magnet off-normal contacts should close the OH lead through to the AMRST, operating relay OH. Relay OH locks and transfers lead OH from its winding to lead HM to the link, operating the AMRST hold magnet L00 in the link.

L1-3.2.6 Cut Off (CO) Test (SFD-L111)

Relay OH transfers the progress indication from lamp OH to lamp CO and closes an operating circuit for relay C in the AMRST. On nonbylink tests, the circuit is over lead CO, through the IRL crosspoint, to ground in the register. On bylink tests, the circuit is to operated contacts of relay BL to ground. Relay C locks, extinguishes the CO progress lamp, and connects lead D from the link to the winding of relay D (SFD-L308).

L1-3.2.7 Release Check (RLK) Test (SFD-L112)

The operation of relay C in the AMRST lights lamp RLK and grounds lead BL through the IRL to the IR operating the CK and in turn the RLK relay. The C relay also causes release of the L0- followed by the ORP- relays in the AMRST along with the link preference relays in the IRL. Operation

of the register RLK relay removes battery from the LK lead releasing relay LK in the AMRST. Removal of this battery also opens the ST lead to the IRL which releases the test preference relay TP00 (SFD-L110). The TP00 relay releases the TCL- relay in the AMRST. The release of relay LK also transfers the progress indication from lamp RLK to lamp WS.

L1-3.2.8 Wink Short (WS) and Wink Long (WL) Tests (SFD-L112,13)

An IR, when seized, must give a wink to the trunk. The wink consists of supplying battery and ground to the trunk with ground on the ring initially and then reversing the polarity after a timed interval. The wink must be long enough to be recognized by the circuit at the originating end of the trunk, and should not be too long because that would waste holding time. In practice the registers give a wink of about 0.160 to 0.350 second. The wink is tested by two timers: WS looks for a wink that is too short, and WL looks for a wink that is too long.

The AMRST relay TG is a double wound polarized relay which tests the polarity of trunk closures. With ground on the ring, its P- contacts operate (3 and 4T, 3 and 4B); when the trunk reverses, its P+ contacts operate (1 and 2T, 1 and 2B). The P- contacts operate relay W, which starts both timers. The WS timer should function and operate relay WS before the trunk reverses; otherwise closure of the P+ contacts will operate relay WS1 as an indication that the wink was too short. After WS operates, the P+ contacts should close and operate wink OK relay WOK before the long timer functions; otherwise relay WL will operate as an indication that the wink was too long. A more detailed description follows.

When relay C operates, as described previously, it connects the T and R leads from the IRL through make-contacts of relays NBL and C to the windings of relay TG. If the IR has ground on the ring and battery on the tip, contacts 3 and 4 of the TG will close and operate relay W. Relay W locks and starts timing by closing charging circuits for capacitors WS and WL. Capacitor WS started from a discharge condition because of a discharge circuit through resistor WS2 and contacts 2 and 3T of W. Its charging circuit is from 135-volt battery through resistor WS, potentiometer WS, capacitor WS, contacts 1 and 2T of W, break contact of WS1, through the winding of relay WS to ground. Since the capacitor is bridged across the control gap (terminals 1 and 4) of tube WS, the tube will fire when the capacitor becomes charged to about 70-volts. When it fires, relay WS will operate on a circuit from 135-volt battery, WS tube main gap (terminals 2 and 4), a make contact of W, a break contact of WS1, and through the winding of relay WS to ground. Potentiometer WS should be adjusted so that relay W, tube WS and relay WS will operate in a period of 125 to 140 ms as covered in the circuit requirements table of SD-25680-01. Relay WS locks to battery through resistor S, which extinguishes the tube (to extend its life) by reducing

the voltage across the main gap to less than 65-volts. If the trunk should reverse too soon, relay TG would operate its 1 and 2 contacts and operate relay WS1, which would lock, discharge capacitor WS before its tube fired, and operate relay TBL. Normally the trunk will reverse after WS operates, operating relay WOK. Should the reversal take too long, tube WL would fire. Capacitor WL charges on a circuit from 135-volts through resistor WL, capacitor WL, make contact of relay W and break contact of relay WOK to ground through the winding of relay WL. After about 370 to 640 ms, the capacitor will become charged to about 70-volts and fire tube WL, which will operate relay WL on a circuit from battery through the tube main gap (terminals 2 and 4), a make contact of W, a break of WOK, and through the winding of relay WL to ground. Relay WL will lock and open the operating circuit of relay WOK. Normally, however, relay WOK should operate first, lock, and discharge capacitor WL before its tube fires. The progress indication is advanced from lamp WS to lamp WL when relay WS operates, and to lamp D when relay WOK operates.

L1-4 TIMING DURING TEST CALLS (SFD-L122,23)

For each test call, a single timing interval of 40 to 70 seconds is provided. If the test is not completed in this period, the timer will function to operate the TBL relay and light the TBL lamp. A time-out will cause a trouble record to be taken with information perforated on the trouble card.

When ONT1 operates at the start of a test call, it operates TMA on its primary winding. Relay TMA removes the TM2 resistor shunt from the TM capacitor and connects ground through the TM relay to the capacitor. The TM capacitor starts to charge in series with the timing resistor TM3. With the TM capacitor discharged, the 1 to 4 control gap of the TM tube will have no potential applied across it. As the capacitor charges, its voltage will be applied across the control gap. When the charge has reached approximately 70 volts, the tube will ionize across its control gap, and current will then flow in the main gap to operate the TM relay.

When TMA operates, it locks on its secondary winding to ground from ONT1. Relay TMB operates through TMA contacts to the same ground and opens the operate circuit of TMA.

In case of number check failure, TRR2 will operate and release TMA and TMB. When TMB releases, TMA and TM2 operate to start a 10- to 17-second timing to cover the trouble record.

If the TM tube ionizes, the TM relay operates. Relay TM operates TMI which locks. The TMI releases TMA and TMB. Relay TMA discharges the TM capacitor and releases TM. Relay TMI operates the TBL relay to indicate trouble. The TBL operates TA to stop the timing which would restart with the reoperation of TMA following release of TMB.

If a trouble record is required, a ground will be connected through a make contact of TMI to operate TRR1. When TM releases, a trouble record will be made as previously described. Relay TBL will not operate until the end of the trouble record. During the trouble record, the timer will function at the 10- to 17-second rate. If a timeout occurs during a trouble record, DL will operate to bring in an alarm and free the MTFC.

SECTION L, PART 2

PULSING

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L2 PULSING

Part L2 describes how the Automatic Monitor Register Sender Test (AMRST) outputpulses into the Originating Register (OR) and Incoming Registers (IR) on register tests and how it receives the outputpulses of the sender on Outgoing Sender (OS) tests.

L2-1 REGISTER TESTS

The following paragraphs describe the operation of the TOUCH-TONE, dial pulse, and multifrequency generators; and the outputpulse steering circuit in the AMRST.

L2-1.1 ORIGINATING REGISTER (OR) TESTING

Now that the Master Test Control (MTC) circuit is connected to the OR via the Originating Test Line (OTL) the AMRST pulses the digits set on the keys or switches of the MTC into the OR where they are recorded and stored.

L2-1.1.1 Preparation for Outputpulsing (SFD-L208)

After the OTL is connected to the OR, the L, SR, and ON1 relays of the OR operate. The operating ground of the ON1 relay is extended to the AMRST on the H lead and operates TAC. Relay TAC operates TAC1 which locks to ON1. Relay TAC1 connects resistance ground through the TAC relay to the H lead to the OR. This ground serves to hold the ON1 relay of the OR if its register operating ground is removed. The TAC relay is a polarized relay which would hold operated to the register ground even when shunted by the TAC1 resistor. However, when the OR attempts to release, as evidenced by removal of ground from the H lead, the current through TAC will reverse, and TAC will release. If TAC releases following the operation of TAC1, TAC2 will operate. This relay arrangement thus permits holding the register off-normal for trouble tracing purposes while at the same time recognizing when the release circuit of the OR functions.

The TAC1 relay operates the ORON. For dial pulsing operation, the POR2 relay will be normal, and operation of ORON will cause the dial pulse generator to begin pulsing into the OR. For TOUCH-TONE operation, the POR2 relay will be operated, and the operation of ORON will operate GA (SFD-L220) which will cause TOUCH-TONE signals to be sent to the register. The OR will be sent the digits set on the key or switches of the MTC circuit.

L2-1.2 INCOMING REGISTER (IR) TESTING

After the incoming register tests have been completed satisfactorily, the AMRST pulses the digits set on the keys or switches of the MTC into the IR where they are recorded and stored.

L2-1.2.1 Preparation for Outpulsing (SFD-L208)

On IR tests, pulsing must await completion of the wink tests. On dial pulse operation the WOK relay operates the dial pulse relay DLP. Relay DLP operates DLP1 which disconnects the tip and ring from relay TG and starts the dial pulse generator.

On multifrequency operation the WOK relay operates the multifrequency relay MFP. Relay MFP operates the go ahead relay GA. The MF generator is now ready to start sending.

L2-1.3 "TOUCH-TONE" PULSE GENERATION

When the TOUCH-TONE features of an OR are being tested, TT pulses are generated by the AMRST and sent to the OR which records them as digits and transfers them to the marker. From there they pass through the Master Test Frame Connector (MTFC) to the AMRST where they are matched against the digits actually transmitted.

In order to test the OR and its associated TT receiver circuit adequately, several types and combinations of pulses can be generated. These are: fast pulses (approximately 11 pulses per second) with long intervals between them, fast pulses (at the same rate) with short intervals between them, slow pulses (approximately 1.0 per second), and pulses under control of a key at any desired rate. The pulses may be transmitted at a normal, high, or low signal level under control of a key. Normal tests send the office code and number. Each digit is comprised of two frequencies, one from a high group of four frequencies and one from a low group of four frequencies. Special tests send a test digit before the office code. These test digits can be comprised of a single frequency from either the high or low frequency group, or the digit 1, 5, 9, or 0 in combination with a 2000 cps frequency.

L2-1.3.1 Pulse Generator (SFD-L221)

The TOUCH-TONE (TT) pulse generator consists of the PG and PG1 relays and the associated capacitors and resistors. Relay PG is a mercury contact relay with two windings. The relay has a single armature spring which closes with two separate front contacts or with two separate back contacts. The relay is polarized so that it can be controlled by current direction, and it is not biased. Consequently, with no current flowing, the armature takes no definite position, and it may remain with the armature closing either the front or the back contacts. The current reversals are under control of the auxiliary relay PG1, which in turn is under control of PG to complete a self interrupter circuit.

When ORP operates, subsequent to the operation of the STT key at the beginning of the test, ORP connects ground through a normal contact of SPB to one side of the PG capacitor and the PGO resistor, thus grounding out the battery and placing ground potential at the -6 terminal of the secondary winding of PG. At this time, the 7 terminal of PG (+ for the secondary winding and - for the primary winding) is connected to resistance battery. The current in the secondary winding is in a direction to release PG, but the current in the primary winding charging the PG capacitor is in a direction to operate PG. Initially the primary ampere turns are controlling, and the relay operates, but as the capacitor becomes charged the primary winding ampere turns decrease. Finally the secondary winding ampere turns become controlling and cause PG to release. The circuit is now prepared for pulsing and remains in this condition until the start TOUCH-TONE pulsing relay, SPB operates (SFD-L223). Relay SPB in operating disconnects ground from the PG capacitor and from the PGO resistor allowing the PGO resistor battery to become effective and connects ground to the 7 terminal of PG through PG1 normal contacts. This causes the current in the secondary winding to flow in a direction to cause operation of PG and sets up a circuit for discharging and charging the PG capacitor in the opposite direction through the primary winding. At first the primary ampere turns are controlling and PG remains unoperated. Then as the capacitor becomes charged, the primary ampere turns decrease and the secondary winding again takes control causing PG to operate. Relay PG, in operating with SPB operated, operates PG1 to again reverse the circuits through both windings, causing PG to release after a timed interval. This cycle is repeated as long as PG1 remains under control of PG. When it is desired to stop the interrupter, the SPB relay is released, thus preventing further operation of PG1 and stopping the interrupter.

The time PG remains on its front and back contacts is controlled by the values of the capacitor and resistors. In the AMRST two sets of constants are provided to give two combinations under control of LGP key. Facilities are provided for adjusting and controlling the output by removing or adding resistance to the circuit networks.

L2-1.3.2 Adjusting TOUCH-TONE Pulse Generator

Two combinations of speed and per cent break are provided for the TOUCH-TONE pulse generator as covered in the circuit requirements table of SD-25680-01. Four adjustments are provided, two for the two pulsing speeds and two for the corresponding percent breaks. The PG2 to PG6 and the PG11 to PG15 resistors control the two pulsing speeds. The PG7 to PG9 and PG16 to PG18 resistors control both of the percent break adjustments. A speed and an associated percent break adjustment are almost but not quite independent; therefore, after changing one, the other should be rechecked. A summary of the pulse times is tabled as follows:

<u>Control Key</u> <u>Operated</u>	<u>Closure of PG1</u> <u>Break Contacts</u>	<u>Open of PG1</u> <u>Break Contacts</u>
-	40 ms	50 ms
LGP	50 ms	40 ms

L2-1.3.3 Assignment of Frequencies (SFD-L226)

The TOUCH-TONE frequencies are generated in the AMRST by means of three transistor oscillators. The "high" frequency oscillator consisting of the TA transistor, LA transformer, and associated apparatus is used to generate any one of four "high" frequencies designated H(1-4) under control of the HF(1-4) oscillator control relays. The "low" frequency oscillator consisting of the TB transistor, LB transformer, and associated apparatus is used to generate any one of four "low" frequencies designated L(0, 3, 6, 9) under control of the LF(0, 3, 6, 9) oscillator control relays. The auxiliary oscillator consisting of the TC transistor, LC transformer, and associated apparatus is used to generate a 2000 cps frequency under control of the SPF relay. The frequencies of the "high" and "low" frequency oscillators in combination are assigned on a 3 by 4 basis (12 button set) or on a 4 by 4 basis (16 button set) to represent the digits 0-9. The frequencies of the "high" and "low" frequency oscillators singly, or in combination with the frequencies of the auxiliary oscillator, are used for special TOUCH-TONE tests as described in Single Frequencies Test and Special Frequency Test.

The output of each oscillator appears in the primary winding of its associated OA, OB, or OC output transformer. The secondary windings of these transformers are multiplied under control of the SPF special frequency test relay and the HF and LF frequency group selection relays to permit the oscillator outputs to be superimposed on each other. When not included in the multiple, the transformer secondary winding is replaced by its associated OA3, OB3, or OC3 resistor so as to maintain a constant line impedance.

L2-1.3.4 Generation of Frequencies (SFD-L227)

The frequencies required for TT calling tests are generated by three bridge stabilized oscillators. Power for operating the oscillators is obtained from the 48-volt supply. The oscillators are prepared to function when ORP operates at the start of an OR TOUCH-TONE calling test.

The transistor in each oscillator operates as an emitter-follower amplifier in which any change in base voltage results in a corresponding change in emitter voltage. The current in the base is in phase with the current in the emitter. Base to emitter bias is maintained across the resistor which is connected to ground when the ORP relay is operated. The amplification obtained from the transistor is sufficient to drive a tuned circuit and therefore it can act as an oscillator. The oscillations are maintained by returning a sufficient portion of the output as an input to the base. This feedback is obtained from the transformer winding in series with the emitter which is inductively coupled to the transformer winding in series with the base. The third winding on the transformer together with a fixed capacitor forms the tuned circuit. Taps are furnished

on this winding which are connected to a fixed capacitor by oscillator control relays. Four taps are provided which permit the oscillator to generate any one of four frequencies. The transformers employ ferrite cup cores with slug tuning for control of the transformer inductance to provide means for precise frequency adjustment at any particular tap. The taps are located at points of exact turns ratios, thereby permitting all the required frequencies to be adjusted within range by a single adjustment.

To prevent overloading of the transistor, the peak amplitude of the oscillations is limited by the varistor in shunt with one section of the tuned winding of the transformer. The potentiometer in each oscillator controls the signal current flowing in the oscillator output transformer thereby providing means whereby the output level of each oscillator can be adjusted.

The "high" frequency oscillator consists of the TA transistor, LA transformer, and associated apparatus and is used to generate any one of four "high" frequencies. Under control of the MXF and MNF relays, the oscillator can also generate frequencies which are above or below the nominal frequencies. The nominal "high" frequencies are generated by forming the tuned circuit with the A01 and A02 capacitors. With the MNF relay operated, frequencies $(1.5 \pm 0.1)\%$ below the nominal frequencies are generated by forming the tuned circuit with the A0(1-3) capacitors. With the MXF relay operated, frequencies $(1.5 \pm 0.1)\%$ above the nominal frequencies are generated by forming the tuned circuit with the A01 capacitor.

The "low" frequency oscillator consists of the TB transistor, LB transformer and associated apparatus and is used to generate any one of four "low" frequencies. Under control of the MXF and MNF relays the oscillator can also generate frequencies which are $(1.5 \pm 0.1)\%$ above or below the nominal frequencies. The frequencies generated are determined by forming tuned circuits with the B0- capacitors in the same manner as the A0- capacitors described above for the "high" frequency oscillator.

The auxiliary oscillator consists of the TC transistor, LC transformer, and associated apparatus and is used to generate a 2000 cps frequency under control of the SPF relay. This "special frequency" signal is generated by forming the tuned circuit with the C01 capacitor connected across winding 1-3 of transformer LC.

To insure that the oscillator output signals are at their proper level at the beginning of each pulse, the oscillators are preexcited by charging the A0-, B0-, and C0- tuning capacitors through the OA6, OB6, and OC6 resistors respectively during the silent interval of pulsing.

The TD transistor (SFD-L226) and associated apparatus is used to reduce the output impedance of the oscillators to provide a low impedance signal source. This low impedance source will maintain a relatively constant signal level input to the circuits under test regardless of their input impedances.

L2-1.3.5 Adjustment of TOUCH-TONE Oscillators

The ADJ, HFA, and LFA keys and the VL jack are provided for the purpose of adjusting the output frequencies and levels of the oscillators.

For the frequency adjustment, a Berkley EPUT meter is plugged into the VL jack to measure the output frequency of each oscillator. Each oscillator is adjusted to oscillate at a single nominal frequency by adjusting the slug tuned oscillator transformer. The adjusting procedure is outlined in Circuit Note 170 of SD-25680-01.

For the level adjustment a volume level indicator is plugged into the VL jack to measure the output level of each oscillator. The PA, PB, and PC potentiometers are provided to adjust the oscillator output levels as covered in Circuit Note 171 of SD-25680-01.

L2-1.3.6 Normal Test

This test is made with none of the pulsing keys or switches of the AMRST operated. Pulses are fast and short with the TOUCH-TONE signals sent at a normal level. The office code and number are sent to the OR. Any digits may be used, but it is desirable to select digits which will check all the TOUCH-TONE frequencies. If digits 3, 5, 7, and 0 are used, all the frequencies used to represent the digits 0-9 will be tested. Pulses are generated by the PG1 relay which is under control of the capacitor timed PG relay.

L2-1.3.6.1 Preparation for Pulsing (SFD-L208)

With the STT and PB keys operated in the AMRST and the OR key operated or TSTA switch set to the OR position in the MTC circuit, the STT relay operates followed by the POR1 and DOR1 in the AMRST. The ORP relay in the AMRST operates furnishing off-normal grounds to the TOUCH-TONE signal generator and oscillators. The ORP also closes a path for holding the OR. Subsequently, when the ST key is operated at the MTC, the ORST relay operates. Relay ORST operates PBP and PB in the AMRST to prepare for TOUCH-TONE signaling. Relay ORST also operates the FD4 relay. The AMRST is now prepared for TOUCH-TONE pulsing.

L2-1.3.6.2 Pulsing Digits (SFD-L220,21)

When the OR is ready to receive TOUCH-TONE pulses, the ORON relay is operated, which in turn operates the GA "go ahead" relay. Relay GA locks and operates the MF5 relay to connect the windings of the (0-9)F frequency control relays to the digit keys at the MTC circuit. Relay MF5 also operates the SPB relay which grounds the steering advance lead to the outsteering circuit to operate the OSA and OSA1 steering relays, assuming A is the first digit to be outpulsed. Relay SPB starts the TOUCH-TONE signal generator as described earlier and also closes the tip and ring signaling path to the OR, but no signal is sent at this time.

After a timed interval the PG1 relay will operate and remove ground from the steering advance lead permitting the BP or KP1 steering relay to release. The release of BP or KP1 connects ground to the AK lead to the MTC through the operated OSA steering relay to the (0-19)F frequency control relays, one of which will operate corresponding to the operated A digit key or switch at the MTC circuit. The operated frequency control relay operates one of the HF(1-4) and one of the LF(0, 3, 6, 9) oscillator control relays. The operated HF(1-4) relay connects the AO-capacitors to the tuned winding of the high frequency oscillator transformer. The operated LF(0, 3, 6, or 9) relay connects the BO- capacitors to the tuned winding of the low frequency oscillator transformer. Connection of these capacitors complete the tuned circuits in the oscillators and cause the oscillators to generate frequencies required for the A digit corresponding to the operated frequency selection relays. The operated oscillator control relays, their corresponding digit assignments, and the frequencies generated are summarized as follows:

<u>Digits or Signals</u>		<u>Operated Oscillator Control Relays and Frequency</u>
<u>12 Button Set</u>	<u>16 Button Set</u>	
0	0	HF2, LF9
1	1	HF1, LF0
2	2	HF2, LF0
3	3	HF3, LF0
4	4	HF1, LF3
5	5	HF2, LF3
6	6	HF3, LF3
7	7	HF1, LF6
8	8	HF2, LF6
9	9	HF3, LF6
P	SPARE	HF1, LF9
SG	A	HF3, LF9
	FO	HF4, LF0
	F	HF4, LF3
	I	HF4, LF6
	P	HF4, LF9

Actual frequencies are as follows:

<u>Operated Oscillator Control Relay</u>	<u>Cycles Per Second</u>
HF1	1206
HF2	1336
HF3	1477
HF4	1633
LF0	697
LF3	770
LF6	852
LF9	941

After a timed interval, the PG1 relay releases to apply the TOUCH-TONE frequencies to the tip and ring. Release of PG1 also replaces ground on the steering advance lead to operate the OSB steering relay. The next operation of PG1 terminates the A digit, and the OSA steering relay is released. The release of OSA removes ground from the AK lead and places ground on the BK lead to the MTC thereby permitting the release of the operated oscillator control relays corresponding to the A digit, and the operation of the relays corresponding to the B digit.

In this manner, the remaining digits are sent one by one. For each digit, the PG1 relay releases to send a pulse and preoperate the next steering relay. After a timed interval, PG1 operates to release the previously operated steering relay and frequency control relay and to operate another frequency control relay. This cycle repeats until all digits have been sent.

L2-1.3.6.3 Final Digit (SFD-L210)

The AMRST is arranged to pulse any number of regular digits from none to eleven depending on how many digit keys are operated at the MTC circuit. When BP operates, it operates final digit relay FD. Each succeeding steering relay, when operated connects the winding of the FD relay to the corresponding row of keys or switches, and if operated, ground is returned to hold FD. When the steering relay corresponding to the last key or switch that is operated is released, the ground is removed allowing the FD1 relay to operate. Relay FD1 opens the circuit to the SPB relay to stop further pulsing and operate relays FDA and FDB which close ground to operate a -7 digit relay as an indication of what digit was pulsed last. The OR should now recognize the end of pulsing.

L2-1.3.7 Long Pulse Test

The normal test produces fast short pulses, each digit pulse being about 0.04 seconds and each open between digits about 0.05 seconds. On the long pulse test, digit pulses are fast and long, each digit pulse being about 0.05 seconds and each open between digits about 0.04 seconds. This test is made by operating the LGP key in the AMRST. In other respects the test is the same as a normal test.

L2-1.3.8 Slow Pulsing Test (SFD-L223)

This test is made with the SLO key in the AMRST operated. It checks that the OR records each digit only once in its proper sequence when pulses are slow and long. The precision TOUCH-TONE signal generator is replaced by two slow relays SP1 and SP2 and the KA, KAA, and SP auxiliary relays.

When the test starts, ground from BP or KP1 operates the SP slow pulse relay which locks (SFD-L220). When the register is ready to receive pulses, GA operates in turn operating MF5. With SP operated, operation of MF5 operates the SP1 relay. This starts a pulsing cycle in which SP1 operates SP2, which releases SP1, which after an interval releases SP2, which reoperates SP1, etc. Every time SP1 operates, it operates KA which operates KAA to apply frequencies to the tip and ring provided a frequency control relay is operated just as PG1 does when pulses are fast. Relay KA also grounds the steering advance lead to operate a new steering relay. Every time SP1 releases, KA releases which releases KAA ending the pulse and removing ground from the steering advance lead to release the previous steering relay. The steering relays operate frequency control relays (0-9) as explained for a normal test. When all digits have been pulsed, relay FDI operates and stops pulsing by opening the operate path of SP1. The OR should respond the same as on tests which are fast pulsing.

L2-1.3.9 DSS Pulsing Test (SFD-L220)

When locating circuit troubles, TOUCH-TONE pulses may be controlled manually instead of by a pulse generator. If AMRST key DDSS is operated, one TOUCH-TONE pulse will be sent each time the ST key of the MTC circuit is operated subsequent to its first operation which starts the test.

Alternatively, a 32A test set may be plugged into a remote control jack of the control circuit and the white button operated once for each pulse. The pulse persists as long as the ST or white button is operated. The white button is arranged to lock for convenience in clearing trouble conditions.

When the test starts, a ground from BP or KP1 operated through the operated DSS key operates the SSP, step-by-step pulsing relay. This relay locks, opens the operate path of SPB and prepares a path for operating KA under control of the RC relay. Relay RC operates from the control circuit when the ST or white button is operated after a test is started (SFD-L219), in turn operating KA which operates KAA to apply frequencies to leads T and R and also operate steering relays as described under slow pulsing tests.

L2-1.3.10 Low and High Level Tests

This test checks the ability of the TOUCH-TONE receiver circuit to function over a fixed range of TOUCH-TONE signal input levels. This test is made with either the Low Level (LLV) or High Level (HLV) key operated. The output level of each TOUCH-TONE oscillator is adjusted to +3 dBm. On normal tests, the oscillator outputs are passed through the low loss LL pad which inserts a 10 dB loss to furnish a -7 dBm signal to the TOUCH-TONE receiver. When the LLV key is operated, the HL pad is placed in series with the LL pad to add an additional 12 dB loss to furnish a -19 dBm signal. When the HLV key is operated, neither pad is inserted in the line and a +3 dBm signal is transmitted. In all other respects, the test is the same as for a normal test.

L2-1.3.11 Maximum and Minimum Frequency Test (SFD-L221)

This test checks the ability of the TOUCH-TONE receiver to function properly when it receives TOUCH-TONE signals comprised of frequencies which are $(1.5 \pm 0.1)\%$ higher or lower than the nominal frequencies. This test is made with the FCB switch in the MXF or MNF positions. When a test is started and the BP or KP1 steering relay is operated, ground will be extended through the FCB switch to operate either the MXF or MNF relays which lock up under control of the PBP relay. When a pair of oscillator control relays is operated and either the MXF or MNF relay is operated, the tuning capacitors are changed in the tuned circuits of the "high" and "low" frequency oscillators, to either raise or lower the nominal output frequencies as described earlier. In all other respects, the test is the same as for a normal test.

L2-1.3.12 Single Frequency Test (SFD-L221)

This test checks the ability of the TOUCH-TONE receiver to ignore signals comprised of a single TOUCH-TONE frequency. When this test is made, a long single frequency pulse is transmitted ahead of the office code and number. The long pulse is sent under control of the slow pulse generator which consists of the SP1, SP2, and SP5 slow relays and the KA and KAA auxiliary relay. These relays replace the precision TOUCH-TONE pulse generator until after the transmission of the single frequency. The test is under control of the FCB switch, and the frequency transmitted is under control of the FCA switch. The FCA switch operated to one of its four positions will cause the transmission of a single frequency from the "high" group of four frequencies

when the FCB switch is in the SFH position, or a single frequency from the "low" group of four frequencies when the FCB switch is in the SFL position. The switch positions and the designation of the frequency transmitted are tabled below.

<u>Switch Positions</u>		<u>Frequencies Transmitted</u>	
<u>FCB</u>	<u>FCA</u>	<u>Designation</u>	<u>Cycles Per Second</u>
SFH	4	H4	1633
SFH	3	H3	1477
SFH	2	H2	1336
SFH	1	H1	1209
SFL	1	L0	697
SFL	2	L3	770
SFL	3	L6	852
SFL	4	L9	941

When the test starts and the BP or KP1 steering relay operates, ground is extended through the SFH or SFL positions of the FCB switch to operate the SF1 relay. Relay SF1 opens the operate path of SPB, prepares a path for operating the SP1 relay, connects ground through the FCB switch to operate either the HF or LF frequency group selection relays, and prepares a path through the FCA switch to operate one of the HF(1-4) oscillator control relays if HF operates, or one of the LF(0,3,6,9) oscillator control relays if LF operates. Relay HF operates with the FCB switch in the SFH position and LF operates with the FCB switch in the SFL position. Relay HF operated opens the "low" frequency oscillator output transformer and replaces the secondary winding with the OA3 resistor. Relay LF operated opens the "high" frequency oscillator output transformer and replaces the secondary winding with the OB3 resistor. The resistors maintain a constant line impedance when one of the oscillators is not in use.

When the OR is ready to receive pulses, GA operates, operating MF5. With SF1 operated, operation of MF5 closes a path to operate the SP1 relay to start the slow pulse generator. This starts a pulsing cycle whereby SP1 operates SP2 which operates SP5. When SP2 operates, it releases SP1 which in turn releases SP2. When SP1 operates, it operates KA which operates KAA to apply the single frequency to the tip and ring as determined by the operated oscillator control relay. Relay KA also grounds the steering advance lead to operate the OSA steering relay. When SP2 releases, KA also releases which releases KAA ending the pulse and removing ground from the steering advance lead to release the BP or KP1 relay which in turn releases the SF1 relay and operates oscillator control relays in preparation for sending the normal A digit as determined by the operated A digit key or switch at the MTC. Release of SF1 partially recloses the SPB operate path which will operate when SP5 releases. Operation of SPB applies the A digit frequencies to the line and starts the precision TOUCH-TONE signal generator. Subsequent pulsing is as described for a normal test.

L2-1.3.13 Special Frequency Test (SFD-L221)

This test checks the ability of the TOUCH-TONE receiving circuit to ignore signals comprised of three frequencies, two of which are a valid combination of TOUCH-TONE frequencies at a normal level (-7 dBm) and the third a frequency above the band of TOUCH-TONE frequencies at a higher level (-6 dBm). For this test, a 2000 cps frequency is used as the third frequency. When this test is made, a long three frequency pulse is sent in the same manner as described for the single frequency test. The test is under control of the FCB switch which is operated to the 3FS position and the FCA switch which is operated to one of the 1 to 4 positions. The switch positions and the designations of the frequencies transmitted are summarized below. The actual frequencies are as shown in the tables in the paragraph on single frequency test.

<u>Switch Position</u>		<u>Frequencies Transmitted</u>
<u>FCB</u>	<u>FCA</u>	
3FS	1	H1, L0, 2000
3FS	2	H2, L3, 2000
3FS	3	H3, L6, 2000
3FS	4	H2, L9, 2000
3FS	5	H4, L9, 2000

When the test starts and the BP or KP1 steering relay operates, ground is extended through the 3FS position of the FCB switch to operate the SPF relay. The SPF opens the operate path of SPB, prepares a path for operating the SP1 relay, and closes the auxiliary oscillator output transformer secondary to the tip and ring leads. Relay SPF also closes a path through the FCA switch to operate one of the HF(1-4) and one of the LF(0,3,6,9) relays which cause one each of the "high" and "low" frequencies to be generated, and connects the CO1 capacitor to terminal 3 of the LC transformer to cause the "auxiliary" oscillator to generate a 2000 cps frequency. Consequently a valid combination of frequencies plus a 2000 cps frequency will be generated simultaneously.

When the OR is ready to receive pulses, the test proceeds in the same manner as for a single frequency test with the SPF relay controlling the test in place of SF1.

L2-1.4 DIAL PULSE GENERATOR

The dial pulse generator provides loop and leak conditions with dial pulse interrupters which, when applied to the pulse counting and recording circuits of the originating and incoming registers, will insure satisfactory operation of these circuits on service conditions. The circuit will dial in rapid succession, or under control of a digit step-by-step key, as many digits as there are keys or switches operated on the code and numerical keys at the MTC.

For testing incoming registers, the IRD relay is operated (SFD-L108) to connect line conditions and dial speeds for checking dial pulse recording features of incoming registers. For testing originating registers, the ORD relay is operated to connect line conditions and dial speeds for checking the dial pulse recording features of originating registers.

L2-1.4.1 Interrupters and Line Conditions (SFD-L222)

Seven keys are provided to control the various line conditions, dial speeds, and percents break. One of these keys must be operated for each dial call. For IR tests with the 24-MAX pps key operated in the AMRST, an additional key, 24X-0, should be left normal for a first test and operated for the second test.

The keys and line conditions are shown on the accompanying table. The register L relay must operate on the loop resistance indicated and release on the leak resistance indicated.

Condition A tests the ability of the register RA relay to hold over dial pulses, and the correctness of the bias winding strength and the adjustment of the L relay.

Condition B tests the ability of the OR SR relay and the IR abandoned call timer to hold over dial pulses and the correctness of the bias winding strength of the L relay.

Condition C tests the ability of the L relay to release long enough to cause a registration in the counting circuit.

Condition D tests the L relay circuit for proper wiring and continuity.

Condition E tests the ability of the L relay to release fast enough to cause operation of RA fast enough to record the first digit in the counting circuit.

Condition F tests the ability of the L relay to provide sufficient front contact closure and to provide sufficient back contact opening to cause proper registration in the counting circuit. It also tests the ability of RA to release and cause registration on digit registers in minimum time between digits.

Condition G tests the ability of the register not to record a false pulse on a surge resulting when a retard coil holding bridge is inserted in the line between digits.

The bridge inserted in the loop on the SURGE test simulates transient conditions which the register L relay meets in service.

For IR tests, the 15 pps interrupters are not used since the other interrupters provide adequate test margins.

ORIGINATING REGISTER NONCOIN TESTS

<u>WS Type Registers Only</u>					
<u>Condi- tion</u>	<u>% Brk</u>	<u>Test Keys</u>	<u>Loop ohms</u>	<u>Leak ohms</u>	<u>Bridge</u>
A	50%	7MIN	2140	5008	None
		7MIN LPO	-	-	-
B	80%	7MAX	2140	5008	None
		7MAX LPO	-	-	-
C	65%	15MIN	-	10,000	Two:2.16 UF isw 274F Indr isw 1620
D	65%	15MAX	300	-	Two:2.7UF isw 274F Indr isw 1620 and One:3.24 UF
E	55%	24MIN	0	30,000	One: 3.24 UF isw 600
		24MAX	1650	None	None
F	70%	24MAX LPO	0	None	None
G	-	Surge	350 then 274B Indr	-	None

Incoming Register TestsWS Type Registers Only

<u>Condi- tion</u>	<u>% Brk</u>	<u>Test Keys</u>	<u>Loop ohms</u>	<u>Leak ohms</u>	<u>Bridge</u>
A	50%	7MIN	4500	16,050	None
		7MIN, LPO	-	-	-
B	80%	7MAX	4500	16,050	None
		7MAX LPO	-	-	-
E	55%	24MIN	0	30,000	One: 3.24 UF isw 600
F	70%	24MAX	4300	-	None
G	-	SURGE	-	2000 then Indr with 20,000 shunt isw 280 relay added	None

L2-1.4.2 Circuit Operation

When a test call is started, ground is connected to the DP lead operating the DP and DP1 relays. Relay DP1 connects the windings of the counting relays 0 to 9 (SFD-L218) to the corresponding levels of the code and numerical digit keys or switches at the MTC circuit for controlling the number of pulses for each digit. Relay DP furnishes off-normal ground and battery to the dialing interrupter relays and operates relays BD1, INT, INT1, PLS, and CTG and releases relays R and S (SFD-L219,22). The PLS relay in operating closes the loop for holding the register. With relay DP operated and R normal, a ground operates the first out steering relay. The circuit is now ready to furnish dial pulses. The number of pulses for each digit will be controlled by the connection of a ground through CTG to one of the 0 to 9 counting relays. This connection is made by the outpulse steering relays and the code and numerical keys or switches of the MTC circuit for the particular digit being dialed.

If a prefix one is to be dialed, the P1 key (SFD-L212), PD1 relay (SFD-L211), or the AP1 key (SFD-L214) in the MTC circuit will be operated to operate either the AD1 or the BP steering relay which will extend the

ground from CTG to the 1 counting relay. If the prefix digits one-one are to be dialed, the P11 key (SFD-L212), the PD11 relay (SFD-L211), or the AP1 and BP1 keys (SFD-L214) in the MTC circuit will be operated to operate the AD or the BP steering relay which will extend ground from CTG to the 1 counting relay. If a prefix digit zero is to be dialed, the PDO relay or the BPU switch, set to position 0, will be operated to operate the AD1 or the AD3 steering relay which will extend ground from CTG to the 0 counting relay. If a prefix digit 9 or 8 is to be dialed, the PD9 or PD8 or the BPU switch, set to position 9 or 8, will be operated to operate the BP or the AD3 steering relay which will extend ground from CTG to the 9 or 8 counting relay.

If the P1 and P11 keys or the PD1, PD11, PD8, PDO, and PD9 relays are normal, or the AP1 and BP1 keys and BPU switch are normal, the OSA steering relay will be operated to connect the ground from CTG to the AK lead to the MTC circuit where it is extended to one of the AA(0-9) leads to the AMRST depending on which button of the A key or position of the A switch is operated (SFD-L217). These 10 leads are extended through the operated GR relay to 10 pairs of counting relays. Relay GR which operates from DOR1 or DIR1 is provided to tie the outputs of the A, B, C, and D keys of the MTC circuit together, and connect them to the counting relays. The outputs of succeeding keys are grouped in the MTC circuit itself.

When the register is ready to receive dial pulses, the SY relay will be operated (SFD-L219). The SY closes ground to cause operation of the counting relay for the first digit, operates the SY1 relay, and starts the release of the capacitor timed relay BD1. The SY relay also removes the test receiver, if one is connected, and removes the tip party ground if a 2-party test is being made. The SY1 removes ground from the lead which operated the first steering relay and provides a ground for the operation of the steering relay for the next digit.

When the SY relay operates to cause a digit to be dialed, ground is removed from the operate winding of the BD1 relay. The BD1 relay is slow-release due to the fact that the current for charging the associated capacitor flows through the operate winding, holding the relay operated until this capacitor becomes partially charged. This slow-release feature measures the interval between digits which are sent in rapid succession for testing the register advances feature.

L2-1.4.3 Interrupter Operation (SFD-L222)

The release of relay BD1 removes ground from the No. 3 terminal of the secondary winding of the INT relay. This ground was shunting the resistance battery supplied through the operated interrupter key. A capacitor is connected from ground to the No. 9 terminal of the secondary winding of the INT relay and removing this shunt ground permits current to start flowing through the secondary winding charging the series capacitor. This current is sufficient to cause the INT relay to release even though its primary winding is energized in the operate direction. However, the relay will

reoperate when the capacitor is charged. The length of time the INT relay remains released depends upon the values of resistance and capacitance in series with the secondary winding and the resistance in series with its primary winding. The magnitudes of the capacitance and resistance are controlled by the speed and per cent break keys. With the INT relay released, the capacitor in series with the secondary winding of the INT1 relay is discharged and, when the INT reoperates, the capacitor starts to charge. The charging current is in a direction to cause the INT1 relay to release. This relay will reoperate, however, when the capacitor becomes charged. With the INT1 relay released, the shunt is reapplied to the resistance battery, and the capacitor in series with the secondary winding of the INT relay is discharged. The discharge current is in the direction to hold the relay operated. When the INT1 relay reoperates, the shunt is again removed from the resistance battery to cause the INT relay to release while current is again charging the associated capacitor. With the INT relay released, the capacitor associated with INT1 is again discharged. Reoperation of INT closes the circuit through the capacitor and winding of the INT1 relay causing INT1 to release. The INT and INT1 relays continue to operate and release as long as the front contact of the BD1 relay is open. The rate of pulsing is dependent upon the key operated. The PLS and CTG relays are controlled from the INT1 contact, releasing when INT1 releases and operating when INT1 operates. Thus the released time of the INT1 relay controls the open period of the interrupter, while the operated time of the INT1 relay, which in turn is dependent on the released time of the INT relay, controls the closed period of the interrupter. The ratio of the open to closed period of these pulses is controlled by the ratio of the released period of the INT1 to the released period of the INT relay. The PLS relay acts as a dial contact and each open of the PLS front contact opens the tip and ring to transmit a pulse to the register.

L2-1.4.4 Counting Relay Connection (SFD-L218)

The front contact of the CTG relay is connected through a make contact of the steering relay OSA, OSB, OSC, etc, whichever one is operated, and through the operated contact of a digit key or switch at the MTC circuit in the corresponding row, to the armature of the prime relay corresponding to the key or switch of the MTC in that row. When the SY relay operates, the counter corresponding to the key or switch of the MTC will be operated. The release of CTG on the first pulse permits the prime relay to operate. The reoperation of the CTG relay operates the next lower-numbered counter. When the CTG releases for the last pulse, which may also be the first pulse if only one pulse is to be dialed for that digit, the 1' relay and BD relay operate. With the BD operated, ground is supplied to the operate winding of the BD1 relay which operates without delay connecting ground to the No. 3 terminal of the secondary winding of the INT relay which prevents the capacitor associated with this winding from starting to charge when the INT1 again operates. When the INT1, PLS, and CTG relays operate at the end of the pulse, they remain operated until the BD1 relay again releases.

L2-1.4.5 Interdigital Interval (SFD-L218)

The operation of the CTG relay at the end of the last pulse operates relays R2 and BD2. Relay BD2 opens the operating circuit of the BD1 relay causing it to release. The BD2 relay also operates relay S. The operation of the S relay is delayed for approximately 50 milliseconds until the associated capacitor has charged. When the surge test is being made, the S relay connects an inductor into the line to produce a surge equivalent to that produced at a switchboard to test the ability of the register L relay to hold operated. The R2 relay connects the discharged capacitor to the secondary winding of relay R causing that relay to operate while the capacitor is charging. The R relay is operated for approximately 100 milliseconds. The operation of relay R opens the steering advance lead permitting the steering relay for the digit just transmitted to release (thus advancing the control leads to the next digit), holds the R2 and BD2 relays, and operates the R1 relay. The R1 relay operated releases all operated counter relays. When the R relay releases, another steering relay is operated to prepare the next circuit for the digit, one digit beyond the next digit to be dialed.

When the BD2 relay operates, it starts the release of the BD1 relay which times the interdigital interval and, when BD1 releases, the cycle is again repeated. The release time of the BD1 relay imposes a time test on the register advance relays. To be most effective this test should be made with the maximum speed and maximum percent break key operated. The release time of the BD1 relay is approximately 180 milliseconds.

The R relay controls the steering relays, operating a relay for the digit one beyond the next digit to be transmitted before dialing each digit and releasing the relay for the digit just transmitted after dialing the digit. For example, before the A digit is dialed, the OSB relay is operated and, after the A digit has been dialed, the OSA relay is released.

L2-1.4.6 Last Digit Indication (SFD-L210)

The originating and incoming registers are arranged for a variable number of digits. The AMRST is arranged to automatically stop dialing when digits are dialed for all of the key or switch positions at a MTC circuit which are operated. Each steering relay, when operated, connects the winding of the FD relay to the corresponding row of keys or switches and, if operated, the FD relay will be operated. When the steering relay corresponding to the last key or switch which operated is released, a shunting ground is removed from FD1 allowing it to operate. Relay FD1 opens the circuit to the SY relay to stop further pulsing and functions to advance the AMRST for checking the release of the register.

L2-1.4.7 Adjustment of Interrupters (SFD-L222)

Facilities are provided by means of 19- and 36- type resistors for adjusting the length of time the interrupter relays are operated and released to control the percentage of make and break periods of the relay contacts to meet the requirements as outlined in the circuit requirements table of SD-25680-01. The following is a list of the resistors used:

Interrupter Resistance Values

Designation	Min (ohms)	Max (ohms)	Steps (ohms)	Associated Relay	Interval	Key
DP1 DP31 DP41	3100	6200	100	INT	Make))	7 pps Min
DP2 DP32	1700	2450	50	INT1	Break)	
DP3 DP33	1400	2950	50	INT	Make))	7 pps Max
DP4 DP34	3500	5050	50	INT1	Break)	
DP5 DP35	797	3388	50	INT	Make))	(15 pps Min (15 pps Max
DP6 DP36	1500	3050	50	INT1	Break)	
DP7 DP37	1000	3050	50	INT	Make))	24 pps Min
DP8 DP38 DP42	270	955	10	INT1	Break)	
DP9 DP39	500	2050	50	INT	Make))	24 pps Max
DP10 DP40 DP43	400	1210	10	INT1	Break)	

Facilities are provided for strapping out any combination of the resistance as may be required for obtaining the pulse speed and percent break as specified in the Circuit Requirements Table. The values of resistances provided are such that the resistances can be increased or decreased in the units shown in the table from the minimum to the maximum value shown. This should be sufficient to obtain the required speed and percent break. Increasing the resistance associated with the INT relay increases the length of the make period of the pulse while increasing the resistance associated with the INT1 relay increases the break period of the pulse.

L2-1.4.8 Digits Step-by-Step (SFD-L219)

The DSS key and DSS relay are furnished in order to permit the transmission of each digit individually. The operation of the DSS key operates the DSS relay to stop the dialing after each digit; dialing is advanced by the momentary operation of the ST key at the MTC circuit. The operation of the ST key operates the RC relay which operates the DA relay and the release of the ST key and RC relay permits operation of relay DA1. The DA1 relay operated connects ground to the SY relay to cause a digit to be dialed in the usual manner. The closure of the SY relay contact short circuits and releases the DA relay but holds the DA1 relay operated. When the R relay contact opens at the end of the digit, the DA1 relay releases and the steering circuit advances for the next digit.

L2-1.5 MULTIFREQUENCY PULSE GENERATION

When a multifrequency IR is being tested, multifrequency pulses are generated by the MF generator and sent to the IR which records them as digits and transfers them to the CM. From there, they pass through the MTFC to the AMRST where they are matched against the digits actually sent.

In order to test the MF IR and its associated MF receiving circuit adequately, several types and combinations of pulses are generated. There are fast pulses (about 10 per second) with short spaces between them, fast pulses (at the same rate) with each pulse of short duration, slow pulses, and pulses sent under control of the speed keys in the AMRST at any desired manual rate. The pulses may be sent at either low level or low loss. A start pulse may be sent at the end of pulsing or omitted, at will. Normal tests send a key pulse KP signal before the first digit; special tests send 2 KP signals, a 3-frequency KP signal before the regular KP signal, a single frequency digit, and a 3-frequency digit.

L2-1.5.1 Normal Test - Low Input

This test is made with no pulsing speed keys of the AMRST operated, with the exception of "start pulse" key STP. Pulses are fast and short, with low input signal strength. Any digits may be used, but it is desirable to select digits which will check all frequencies. For example, digits 3 and 4, with a start pulse will check all frequencies, digit 3 checking frequencies 1 and 2, digit 4 checking frequencies 0 and 4, and the start pulse checking frequencies 7 and 10. If no start signal is used, a digit should be included using frequency 7, such as the digit 7. Pulses are generated by capacitor-timed relay MF1, which is followed by auxiliary relays MF2, MF3, and MF4.

L2-1.5.2 Preparation for Pulsing (SFD-L220)

After the ST key, SRT1 and N1 relay in the MTC operates, the BT2 relay operates which operates STK. Relay STK supplies several off-normal grounds, one of which operates relay FD4 (SFD-L210). Another STK ground is connected through a break contact of relay GA to operate the first out pulse steering relay KP (SFD-L212). Relay KP locks and provides a ground through break contacts of several keys to operate relay KPS. Relay KPS locks to KP, operates relay KPS1, and operates pulse reversal relay PR. Relay PR releases relays MF1, MF2, MF3, and MF4 (SFD-L223). Relay MF2, MF3, and MF4 are polarized relays without biasing springs and the position of the armature is controlled by the direction of current in the single winding. With ground connected to the + terminal and negative battery connected to the - terminal, the armature closes the front or No. 2 contact. With ground connected to the - terminal and negative battery connected to the + terminal, the armature closes the back or No. 3 contact. Relay MF1 has no biasing spring, but the position of

its armature is controlled by the flux from the currents in both the primary and secondary windings. The circuit is from ground, through a make contact of relay FD4, make of PR, break of FMF, primary winding of MF1 from negative to positive, make of PR, windings of MF4, 3, and 2 from negative to positive, make of PR, to resistance battery through a make contact of KPS. It should be noted that capacitor MF is discharged at this time because of a circuit through the secondary winding of relay MF1 and a break contact of relay FMF. With relays MF1 to MF4 released and with the FD4, KP, KPS, KPS1, and PR relays operated, the circuit is prepared to generate MF pulses.

L2-1.5.3 Key Pulse Signal (SFD-L214)

The register is seized and the test progresses through the wink test as described in SCD-L1.3. Then, after WOK operates, MFP operates, which operates the "go ahead" relay GA (SFD-L220) which locks. Operated GA operates relay MF5 which operates relay FMF (SFD-L223). Relay GA also opens the operating circuit of relay KP. The KP remains locked to ground at the STK relay. Relay FMF removes ground from the negative end of the MF1 primary winding. Since battery is tied to this point through resistor MF1, the MF1, 2, 3, and 4 relays are now energized in the operate direction from this battery through the primary winding of MF1, make contact of PR, windings of MF4, 3, and 2, make contact of PR, resistors MF10, 9, 8, 3, 5, 6, and 7 via make contacts of relay KPS, make contacts of PR and FD4 to ground. The make contact of relay MF1 and the MF1 resistor are taken through break contacts of relay SP, but these contacts serve only to provide insulating points when adjusting relay MF1. It should be noted that spring 2B of relay PR is connected to a voltage divider circuit consisting of resistors MF2 through 7 and is connected to both battery and ground. With relay PR operated, this voltage divider (which may be considered a source of 24-volt battery) is connected to the positive ends of relay MF1, 2, 3, and 4. Since their negative ends are connected to battery through resistor MF1, the relays will be energized in the operate direction normally but may be released by merely grounding out resistor MF1.

The operation of FMF, by removing ground from resistor MF1, allows relays MF2, 3, and 4 to operate immediately, but the operation of MF1 is delayed because relay FMF opens the discharge circuit of capacitor MF causing the secondary winding of relay MF1 to be energized in the nonoperate direction by current which now flows into the capacitor from battery through resistor MF1. This current holds relay MF1 down until the capacitor becomes nearly charged. In the meantime, the operation of relay MF4 grounds the steering advance lead operating the second steering relay KP1 (SFD-L214). Relay KP1 locks and transfers the locking circuit of relay KP from off-normal ground to the steering advance lead so that both KP and KP1 remain operated. Most of the contacts of relay KP1 are ineffective as long as KP is operated. Relays MF2 and 3 operate with MF4, but have no function during this interval except on special tests described later.

When the capacitor charging current decreases to a low value, the secondary winding of MF1 loses control, and the relay operates on its primary winding. Its operation grounds out the battery from resistor MF1, reversing the current flow through the primary winding of MF1 and the windings of MF2, 3, and 4 and closing a discharge path for the MF capacitor. Relays MF2, 3, and 4 release immediately, but the release of MF1 is now delayed by the capacitor discharge current which flows in the secondary winding in a direction to keep the relay operated. The release of MF4 opens the steering advance lead, releasing relay KP, which opens the operate path of KPS and closes ground to operate key pulse frequency cut-in relay KPF to prepare for sending a KP signal (SFD-L220).

When capacitor MF becomes nearly discharged, the primary winding of relay MF1 takes control and the relay releases. This reverses the current in the primary winding of MF1 and the windings of MF2, 3, and 4. The operation of MF1 is delayed, but MF2, 3, and 4 operate immediately. Relay MF4 again grounds the steering advance lead, operating bypass steering relay BP, which locks and transfers the locking circuit of relay KP1 to the steering advance lead. Relay BP also operates the FD3 relay as described later under "final digit."

Relay MF2 and 3 connect ac signals over leads T10 and T2, respectively, from the MF current supply circuit, through front contacts of relays KPF and FMF to the primary winding of the AC repeat coil. The secondary winding is connected through a break contact of relays TWT and LL, through pad C and capacitors T and R to the T and R leads to the IRL and thence to the MF register and MF receiving circuit associated with the IR under test. The two frequencies 2 and 10 should be recognized by the receiving circuit as a "gate opener" or "key pulse" signal, whereupon the receiver should ready itself to accept other combinations of frequencies (SFD-228,29).

When relay MF1 operates, it starts discharging the MF capacitor and grounds out the battery through resistor MF1 releasing relays MF2, 3, and 4 at once. Relay MF2 and 3 terminate the KP signal while MF4 opens the steering advance ground, releasing the KP1 relay which releases relays KPF and KPS. The release of KPS puts an auxiliary ground on resistor MF1 through a make contact of relay KPS1 and starts to release relay KPS1 which is slow-release. Relay KPS also releases relay PR. The release of PR reverses the current through the windings of relays MF2, 3, and 4, operating them. The MF2 and 3 have no function at this time, but the operation of MF4 operates the OSA steering relay which locks and transfers the locking circuit of relay BP to the steering advance ground.

When the MF capacitor has become sufficiently discharged, relay MF1 releases, but this has no effect because its front contact is still grounded through the make contact of relay KPS1. When KPS1 releases, current again flows from the battery through the MF1, 2, 3, and 4, but since relay PR has released, the current tends to operate MF1 while it immediately releases MF2, 3, and 4.

L2-1.5.4 Code and Other Digits (SFD-L220)

When relay KPS1 releases after the KP signal has been sent, the release of relay MF4 releases the BP relay. This grounds lead AK to the MTC circuit, where the ground passes through the A digit key or switch of the MTC to one of leads AA (0-9), depending on what number is to be sent (SFD-L217). The ground is connected through the operated GR relay to operate one of the frequency cut-in relays (0-9)F corresponding to the A digit to be pulsed. The MF capacitor starts charging when relay KPS1 releases. When it is nearly charged, relay MF1 operates, operating relays MF2, 3, and 4. Relays MF2 and 3 apply two frequencies to the tip and ring corresponding to the desired A digit which are transmitted to the signal receiver in the IR (SFD-228,29). Frequency combinations are summarized in the following table (note that the numerical frequency designations may be added to obtain the corresponding digit for digits 1 through 9):

<u>Digit</u>	<u>Frequencies</u>
0	4, 7
1	0, 1
2	0, 2
3	1, 2
4	0, 4
5	1, 4
6	2, 4
7	0, 7
8	1, 7
9	2, 7
KP	2, 10
ST	7, 10
Single Frequency	1
3 Freq KP	1, 2, 10
3 Freq Digit	1 plus A digit freqs

Actual frequencies are as follows:

<u>Designation</u>	<u>Cycles per Second</u>
0	700
1	900
2	1100
4	1300
7	1500
10	1700

The operation of MF4 operates relay OSB. The ground which operated MF2, 3, and 4 also started discharging capacitor MF, after which relay MF1 releases, in turn releasing MF2, 3, and 4. This terminates the A digit pulse and releases relay OSA, which transfers the ground from lead AK to lead BK. This releases the frequency cut-in relay (0-9)F which corresponded to the A digit and operates the same or a different one for the B digit.

In this manner the remaining digits are sent one by one. For each digit; relay MF1 operates, MF2, 3, and 4 operate to send a pulse and preoperate a new steering relay, the capacitor discharges enough to release relay MF1, followed by MF2, 3, and 4 release to end the pulse and release the old steering relay, one of the relays (0-9)F releases and another operates, the capacitor charges enough to let MF1 reoperate, and the cycle repeats.

L2-1.5.5 Final Digit (SFD-L210)

The AMRST is arranged to pulse any number of regular digits from none to eleven depending on how many digit keys or switches are operated in the MTC circuit. Assume that only four digits are to be pulsed on this test. When relay BP operates, it operates "final digit" relay FD3 on a path from battery through its winding and break contact, make contacts of relays MF and BP to ground. Relay FD3 locks and transfers the holding circuit of the operated FD4 relay to the ground from the make contact of relay BP. When the next steering relay AD, AD1, or OSA has operated and the BP relay has released, the holding circuit of relay FD4 is transferred from ground on a contact of BP over lead A to the MTC circuit, where there will be ground if an A digit key or switch is operated. Similarly, as pulsing progresses, the holding circuit of relay FD4 is transferred to the other digit keys or switches in the control circuit. Assuming that only four digits are to be pulsed, the E digit key or switch will be unoperated. Therefore, at the end of the D digit, the release of relay MF4 will release relay OSD which will open the operating path of FD4 allowing it to release. Assuming that no start pulse is to be sent, relay STP will be normal. In this case, the release of relay FD4 will stop all pulsing immediately by removing the ground which operates the MF1, 2, 3, and 4 relays. It also releases relay FMF. Ground through a break contact of FD4 operates relay FDA and FDB, which operate a -7 register relay as an indication of what digit was pulsed last. In our example, since relay OSE is operated, relay E7 is operated (SFD-L217), indicating that the last digit pulsed was D. The IR should now recognize the end of pulsing and ground the D lead as described under Disconnect (D) Test L3-2.1.

L2-1.5.6 Start Pulse

For multifrequency incoming registers equipped to require a start pulse before seizing the CM, a start pulse must be transmitted regardless of the number of digits, and the STP key should be operated.

Multifrequency incoming registers may be equipped to seize the marker when the last equipped digit is registered. If the number of digits pulsed is equal to the maximum number for which the register is equipped, the register does not need any start pulse and should ignore it if sent. Tests may be made both with and without the start pulse. However, if less than this maximum number of digits is pulsed, the IR requires a start pulse in order to recognize the end of pulsing. When a start pulse is to be sent after the last digit, key STP should be operated.

If key STP in the AMRST is operated, pulsing does not stop when relay FD4 releases as described under "final digit" because of the ground from a break contact of relay FD6 through a make contact of the STP relay (SFD-L223). Relay FD4 connects leads T7 and T10 from the multifrequency current supply circuit to the contacts of relay MF2 and MF3 so that a start pulse is sent on their next operation (SFD-L229). Relay FD4 also transfers the front contacts of relay MF4 from the steering advance lead to the winding of FD5 so that, when MF4 reoperates, it operates FD5. Relay FD5 locks and supplies a ground which operates FD6 as soon as MF4 releases. Relay FD6 stops all pulsing. The IR should recognize the end of pulsing and ground its D lead.

L2-1.5.7 Number of Digits

Multifrequency incoming registers that are arranged to always require the start signal before seizing the marker also have a feature for detecting certain attendant errors and for giving the marker a reorder indication in such cases. This feature reduces the number of trouble indicator cards caused by these errors. These incoming registers are wired so that a marker start without a reorder indication is possible only if the start pulse occurs in a definite position on certain classes or in or after a definite position for other classes. The terminating 4-digit trunk classes OA, OAS, OB, and OBS always require exactly 4 digits and a start pulse in other than the fifth position should result in a reorder indication by the incoming register. The terminating 5-digit trunk classes AB and ABS always require exactly 5 digits, and a start pulse in other than the sixth position should result in a reorder indication by the IR.

For regular tests, the STP key must be operated and for classes OA, OAS, OB, and OBS, four digits must be used. For classes AB and ABS, five digits must be used.

In order to check that the IR functions properly to give the reorder indication to the CM if the number of digits does not match the class, other numbers of digits should be used and the RRO key should be operated to check the reorder indication. Less than or more than four digits should be used on the 4-digit class, and less than or more than five digits should be used on the 5-digit class.

L2-1.5.8 Pulse Reversal Test (SFD-L220)

The "normal test" produces fast short pulses, each digit pulse being about 0.034 seconds and each open between digits about 0.066 seconds. On the "pulse reversal test," digit pulses are fast and long, ie, pulses of about 0.066 seconds and opens of about 0.034 seconds. This test is made by operating key PR.

The test proceeds through the KP signal as on a normal test up to the point where relay KPS releases. On a normal test, this releases relay PR, which reoperates MF2, 3, and 4, but on this test PR locks to key PR and MF2, 3, and 4 remain unoperated until relay KPS releases. Thereafter, every time MF1 operates, it releases MF2, 3, and 4, and when it releases, it operates them. In other respects the test is the same as a normal test.

L2-1.5.9 Adjusting Multifrequency Interrupter

Two combinations of speed and percent break are provided for the MF interrupter as covered in the circuit requirement table of SD-25680-01. When sending KP signals, the contacts of relays MF2, 3, and 4 must be closed longer than four digits in order to satisfy the MF receiving circuit. Four adjustments are provided, two for the two pulsing speeds and two for the two corresponding percents breaks. A speed adjustment and an associated percent break adjustment are almost but not quite independent; therefore after changing one, the other should be rechecked. A summary of the pulse times is shown in the following table:

Control Relays Operated	Approximate Closure of MF2, 3 and 4 Front Contacts	Approximate Open of MF2, 3 and 4 Front Contacts
KPS, PR	63 ms	47 ms
PR	66 ms	34 ms
-	34 ms	66 ms
SP	400 ms	400 ma

L2-1.5.10 Slow Pulsing Test

This test is made with key SLO operated. It checks that the IR records each digit only once, in its proper position, when pulses are slow and long. This precision MF interrupter circuit including relays MF1, 2, 3, and 4, KPS, KPS1, PR, and FMF is replaced by two slow relays SP1 and SP2 and auxiliary relays SP and KA.

When the test starts, ground from STK operates the KP relay. Relay KP operates slow pulse relay SP which locks. When the wink tests have been completed, relay GA operates, which operates relay MF5, which operates relay SP1. This starts a pulsing cycle in which SP1 operates SP2, which releases SP1, which releases SP2, which reoperates SP1, etc. Every time SP1 operates, it operates relay KA which applies MF frequencies to the T and R leads provided a frequency cut-in control relay is operated, just as relays MF2 and MF3 do when pulsing fast. Relay KA also grounds the steering advance lead to operate a new steering relay. Every time SP releases, KA also releases, ending the pulse and ungrounding the steering advance lead, thereby releasing the old steering relay. The steering relays operate frequency cut-in relays KPF, (0-9)F, etc as explained for a normal test. When all digits have been pulsed, relay FD4 releases and either stops pulsing by opening the operating circuit of SP1 or else, if the STP key is operated, sends a start pulse, after which relay FD6 stops pulsing. The IR should respond the same as on tests which use fast MF pulsing.

L2-1.5.11 DSS Pulsing Test

When shooting trouble, MF pulses may be controlled manually instead of by an interrupter. If key DSS is operated, the MF pulse will be sent each time the ST key of the MTC circuit is operated (subsequent to its first operation which starts the test).

Alternately, a 32A test set may be plugged into a remote control jack of the control circuit and the white button operated once for each pulse. The pulse persists as long as the ST or white button is operated. The white button is arranged to lock for convenience in clearing trouble.

When the test starts, ground through the KP relay and the DSS key operated operates relay SSP. This relay locks, opens the operating circuit of relay FMF, and closes a circuit for operating relay KA from ground on a contact of relay RC. Relay RC operates from the control circuit when the ST or white key is operated after a test has started, in turn operating relay KA, which applies frequencies to leads T and R and also operates outpulse steering relays as described under Slow Pulsing Test.

L2-1.6 OUTPULSING STEERING (SFD-212-15)

The outpulsing steering circuit is provided for connecting the relays which control the number of pulses dialed in the case of dial registers or the particular frequencies transmitted in the case of multifrequency or TOUCH-TONE registers to the proper key or switch at the MTC circuit. The circuit also provides a final digit indication which is used as a stop pulsing signal for dial and TOUCH-TONE register tests and for transmitting the start signal for multifrequency register tests. One steering relay is provided per digit A to H and J to L plus an end relay OSM. The AD, AD1, AD3, AD4, KP, KP1, and BP are provided in addition for use when digits or signals are to be transmitted ahead of the A digit. The MF relay will be operated when the circuit is used in connection with a multifrequency IR test. The PB relay will be operated when the circuit is used in connection with a TOUCH-TONE OR test.

L2-1.6.1 Operation With Dial Pulse Registers

When a Dial Pulse (DP) register test is started, an off-normal locking ground will be supplied for the steering relays through ORST or STK operated (SFD-L215). In addition, a ground from DP operated through R and SY1 normal will cause the operation of the steering relay to which it is connected as controlled by the P1/P11 key (SFD-L212) or the PD1, PD11, PDO, and PD8 relays (SFD-L213) or by the AP1 key, APU switch, BP1 key, BPU switch and CPU switch (SFD-L214) in the MTC circuit. If no prefix digits are to be dialed, these will be normal, and the OSA and OSAL relays will operate. Relay OSA in operating opens its operating circuit and locks through the break contact of OSB (SFD-L215). Relay OSA steers the pulsing control ground through CTG relay to the AK lead to the MTC circuit for controlling the number of pulses to be dialed in accordance with the A digit key or switch operated (SFD-L216,17). Relay OSAL lights the OSA lamp. Before the dialing of the A digit is started, the operate path of the OSA relay is opened and a steering advance ground is supplied from DP through R normal and SY1 operated. This ground causes operation of the next steering relay, OSB in this case, which locks through the break contact of the next steering relay, OSC, and transfers the locking circuit of the OSA relay to the steering advance ground. When the A digit is dialed, the steering advance ground will be opened, allowing release of the OSA relay which enables the contacts of the OSB relay and lights the OSB lamp. Before the B digit is dialed, the steering advance ground is again closed to operate the OSC relay in preparation for the C digit. The circuit progresses in this manner for each steering advance ground pulse.

L2-1.6.2 Operation with Multifrequency Incoming Registers

On multifrequency incoming register tests, the MF relay is operated. When a multifrequency incoming register test is started, an off-normal locking ground will be supplied for the steering relays through STK operated (SFD-L215). Relay STK also extends a ground through MF to cause the operation of KP. Relay KP opens its operating circuit and locks through the break contact of the KP1 relay. Prior to the interval for the transmission of the first signal to the register (KP signal in most cases), the ground which operated KP is opened, and a steering advance ground is supplied through FMF, FD4, and MF operated to operate the next steering relay KP1. When the first signal is transmitted, the steering advance ground is opened allowing release of the KP relay which enables the contacts of the KP1 relay. A reapplication of the steering advance ground will operate the BP relay in preparation for the next pulse. The BP relay is provided to allow an interval after the KP pulses are transmitted for changing the interrupter constants. The next pulse will operate the AD, AD1, AD3, AD4, or OSA depending on the P1/P11 key (SFD-L212) or the PD1, PDO, and PD11 relays (SFD-L213), or the APU, BPU, and CPU switches (SFD-L214) in the MTC circuit.

L2-1.6.3 Operation with TOUCH-TONE Originating Registers

On TOUCH-TONE register tests, the PB relay is operated. When a TOUCH-TONE register test is started, an off-normal locking ground will be supplied for the steering relays through ORST operated (SFD-L215). Relay ORST also closes a ground through POR2 and PB operated to the BP or KP1 relays.

With option X (SFD-L212), BP operates and locks to AD, AD1, or OSA depending upon the position of the P1/P11 key. Prior to the transmission of the first signal to the OR, the ground which operated BP is opened by a break contact of GA. When pulsing is started, a steering advance ground is supplied through PG1 normal, SPB operated, and MF normal. With the P1/P11 key normal, this ground will operate OSA. At the end of the first pulse from the TOUCH-TONE pulse generator, the steering advance ground is opened allowing BP to release which enables the contacts on the OSA relay. Subsequent closure of the steering advance ground will operate the succeeding steering relay, and removal of the steering advance ground will release the preceding steering relay. The circuit progresses in this manner for each closure of the steering advance ground.

With option Y (SFD-L213), KP1 operates and locks through break contacts of BP, AD, AD1, and OSA. Prior to the transmission of the first signal to the OR, the ground which operated KP1 is opened by a back contact of GA. When pulsing is started, a steering advance ground is supplied by PG1 normal, SPB operated and MF normal. This ground will operate BP, AD, AD1, or OSA under control of the PD9, PD8, PD11, PDO, and PD1 relays. With the PD switch in the off position, these relays will be normal, and OSA will operate. At the end of the first pulse from the TOUCH-TONE pulse generator, the steering advance ground is opened allowing KP1 to release which enables the contacts of the OSA relay. Subsequent closure of the steering advance ground will operate the succeeding steering relay, and removal of the steering advance ground will release the preceding steering relay. The circuit progresses in this manner for each closure of the steering advance ground.

With option Z (SFD-L214), KP1 operates and locks through break contacts of BP, AD, AD1, AD3, AD4, and OSA. Prior to transmission of the first signal to the OR, the ground which operated KP1 is opened. When pulsing is started, a steering advance ground is supplied by PG1 normal, SPB operated, and MF normal. This ground will operate BP, AD, AD1, AD3, AD4, or OSA under control of the AP1 key, APU switch, BP1 key, BPU switch, or CPU switch of the MTC circuit respectively. If all are normal, the OSA relay will be operated. At the end of the first pulse from the TOUCH-TONE generator, the steering advance ground is opened allowing KP1 to release which enables the contacts of the OSA. Subsequent closure of the steering advance ground will operate the succeeding steering relay, and removal of the steering advance ground will release the preceding steering relay. The circuit progresses in this manner for each closure of the steering advance ground.

L2-1.6.4 Prefix Digits

The AMRST is arranged to transmit prefix digits in a number of different ways according to the particular options furnished. Three possible arrangements are depicted in the SFD. A description of the three arrangements can be found in the following paragraphs.

L2-1.6.4.1 P1 and P11 Keys - Option X (SFD-L212)

The P11 key is provided for transmitting the prefix one-one ahead of the A digit, and its operation inserts the AD and AD1 relays in the operating sequence ahead of the OSA relay.

The P1 key is provided for transmitting a single "one" ahead of the A digit, and its operation inserts the AD1 relay in the operating sequence ahead of the OSA relay.

L2-1.6.4.2 PD Switch - Option Y (SFD-L213)

The PD switch and the PD0, PD1, PD11, PD8, and PD9 relays are provided for transmitting various prefix digits ahead of the digit set on the A digit key or switch at the master test control circuit. The PD- relays, when operated, insert additional steering relays in the operating sequence ahead of the OSA relay. The relays which are operated and the prefix digits transmitted for each position of the PD switch are tabulated as follows:

<u>PD Switch Position</u>	<u>PD Relays Operated</u>	<u>Prefix Digits Transmitted</u>	<u>Additional Steering Relays Operated</u>
Off	None	None	None
0	PD0	0	AD1
1	PD1	1	AD1
11	PD11	11	AD,AD1
9	PD9	9	BP
90	PD9,PD0	90	BP,AD1
91	PD9,PD1	91	BP,AD1
911	PD9,PD11	911	BP,AD,AD1
8	PD8	8	BP

If the circuit is arranged to function with originating registers which accept 10-digit calls which are preceded by 0-1 or 0-1-1 and prefix digits are not under control of the MTC circuit, the above table is modified as follows:

<u>PD Switch Position</u>	<u>PD Relays Operated</u>	<u>Prefix Digits Transmitted</u>	<u>Additional Steering Relays Operated</u>
Off	None	None	None
0	PDO	0	BP
01	PDO,PD1	01	BP,AD1
011	PDO,PD11	011	BP,AD,AD1
1	PD1	1	AD1
11	PD11	11	AD,AD1
9	PD9	9	BP
90	PD9,PDO	90	BP,AD1
91	PD9,PD1	91	BP,AD1
911	PD9,PD11	911	BP,AD,AD1
8	PD8	8	BP

L2-1.6.4.3 APU, BPU, CPU, Switches in MTC - Option Z (SFD-L214)

The prefix digits are under control of keys and switches in the MTC circuit. These digits are transmitted ahead of the A digit. The keys and switches operated insert additional steering relays in operating sequence ahead of the OSA relay. The relays which are operated and the digits transmitted for each key or switch operated are tabulated as follows.

<u>Key(s) Operated</u>	<u>Switch(s) Operated</u>	<u>Position(s)</u>	<u>Prefix Digits Transmitted</u>	<u>Additional Steering Relays Operated</u>
None	None	Off	None	None
None	BPU	0	0	AD3
AP1	None	Off	1	BP
AP1,BP1,11	None	Off	11	BP,AD1
None	BPU	9	9	AD3
None	APU,BPU	9,0	90	AD,AD3
None	APU,BPU	9,1	91	AD,AD3
11	APU,BPU,CPU	9,1,1	911	AD,AD3,AD4
None	BPU	8,	8	AD3
11	APU,BPU,CPU	8,1,1	811	AD,AD3,AD4

L2-1.6.5 DSS Key (SFD-L219)

The DSS key is provided to permit the digits to be transmitted singly. Its operation causes operation of the DSS relay, RSS relay, or the SSP relay to require the operation of relay RC for the transmission of each digit. The RC relay is operated from the ST key at the MTC circuit or from the white button of the 32A test set.

L2-1.6.6 Last Digit Indication (SFD-L210)

When the steering relay corresponding to the last digit key or switch operated at the MTC is released, a shunting ground is removed from the FDI relay allowing it to operate. The FDI operates the FDA and FDB relays which operates one B-M7 relay corresponding to the last steering relay operated as a last digit indication (SFD-L217).

L2-2 SENDER TEST

The following paragraphs describe the operation of the trunk tests and dial pulse and multifrequency amplifying and repeating circuits.

L2-2.1 SENDER (SDR) TEST

After the OS receives the start pulse signal from the AMRST the digits stored in the OS are outpulsed into the AMRST via the sender M relay where they are recorded and stored.

L2-2.1.1 Preparation for Pulse Receiving (SFD-L208)

After the OS ON relay is operated its operating and locking ground is extended on the H lead to the AMRST where it operates the TAC relay. Relay TAC operates TAC1 which locks to ONT1. Relay TAC1 connects resistance ground through the TAC relay to the H lead to the sender. Application of this ground is delayed until the MT relay releases to prevent interference with the marker check of the sender ON relay locking ground. When applied, this ground serves to hold the ON relay of the OS if its sender operating ground is removed. The TAC relay is a polarized relay which will hold operated to the sender ground even when shunted by the TAC1 resistor. However when the OS attempts to release, as evidenced by removal of ground from the H lead, the current through TAC will reverse and TAC will release. If TAC releases following operation of TAC1, TAC2 will operate. This relay arrangement thus permits holding the OS off-normal for trouble tracing purposes while at the same time recognizing when the release circuit of the sender functions. Relay TAC1 connects ground to operate TK1 (SFD-L238) as an indication that the OS has been connected to the trunk and is starting trunk test timing.

L2-2.1.1 Trunk Test - Off-Hook to On-Hook Supervision

The multifrequency and dial pulse senders, on certain classes of calls, are arranged to accept a change from off-hook to on-hook supervision as a start pulsing signal. This type of supervision is applied to the multifrequency sender with the sender CL2 relay normal and to the DP sender with sender CL3 relay operated. The test consists of checking that the sender introduces a minimum delay but does not exceed a maximum delay in closing the outgoing tip and ring to the sender supervisory relays as well as checking that the OS recognizes the start pulsing signal.

When the OS is selected by the MTC circuit, the DOS2 or MOS2 relay operates in turn operating the ONS relay. When the trunk used on the test is connected to the OS by the OSL circuit, the ground for operating the sender ON relay is extended through the sender M relay to operate relay TAC of the AMRST (SFD-L208). Relay TAC operates TAC1 which in turn operates TK1 (SFD-L238). Relay TK1 lights the TK1 lamp and closes the TO and RO leads from the OS via the OSL, trunk, and Trunk Link (TL) circuits to the windings of the TK relay (SFD-L239). Relay TK1 also starts the TMN and TMX timers. Relay TMN requires approximately 450 milliseconds for operation and checks the minimum interval. Relay TMX requires approximately 1050 milliseconds for operation and checks the maximum interval. The OS must close the trunk tip and ring so as to operate the AMRST TK relay after TMN operates but before TMX operates or the trouble relay TB2 will operate to block the test. Relay TB2, if operated, will operate the TBL relay to light the TBL lamp.

If TK operates after TMN and before TMX, it operates TG1 (SFD-L238). Relay TG1 locks, lights the TK lamp, and opens the circuit to the TG2 relay which was operated from DPST or MFST. Relay TG2 is slow-release to simulate a link delay at a distant office which would extend the initial on-hook interval. Relay TG1 also stops the TMX timer to prevent false operation of the TB2 relay. When TG2 releases, it causes operation of TG3 to reverse the polarity of the TO and RO leads. Relay TG3 also starts the RV timer which times an interval of trunk reversal or off-hook supervision of approximately 85 milliseconds (SFD-L241). Relay RV operates at the end of the time interval and restores the TO and RO lead to the original polarity. The OS should recognize this change as a start pulsing signal and should start pulsing.

L2-2.1.3 Trunk Test - On-Hook Supervision

The dial sender is arranged, when working with step-by-step trunks, to recognize on-hook supervision as a start dialing signal. This feature is tested with class relays CL2 and CL3 normal.

Relay TK1 is operated from ONS and starts the TMN and TMX timers in the usual manner. Relay TK must not operate before TMN but must operate before TMX, or TB2 will be operated. For this test, the time of the TMN timer is increased to approximately 540 milliseconds. If TK operates at the proper time, TG1 will be operated to light the TK lamp; but immediately following this, PL will be operated to extinguish the TK lamp and light the PL lamp as an indication that the OS recognized the on-hook supervision as a start dialing signal.

L2-2.1.4 Dial Pulse Amplifier and Repeater (SFD-L230)

This circuit is used to repeat dial pulses received from OS. It, in conjunction with the L relay, performs the functions of the L relay in the terminating equipment at the distant office. In order that these functions be performed with a minimum of interference to the pulsing relays in the sender, the connection is made at a high input impedance. Since the high impedance circuit does not pass sufficient power to operate a relay directly, an amplifier is used to transform voltage changes occurring across selected portions of the service circuit during pulsing into changes in power of sufficient magnitude to operate a pulse repeating relay.

The conditions obtained during pulsing for an OS are different from that for registers. The voltage drop across the contact or contacts controlling pulsing is zero or less (potential reversed) when the circuit is closed. When the pulsing circuit is opened at the sender, the voltage across the tip and ring rises to the value of the office battery potential at the distant office. The voltage to ground from either conductor may be altered by ground potential conditions existing between offices. To meet these conditions, an amplifier, ungrounded except for the paths obtained over tip and ring, and with a fixed bias of moderate value, is used.

To prevent recording as a legitimate pulse a surge occurring due to switching conditions in PBXs and DSA boards, a blocking circuit is provided. Pulses shorter than this timed value are rejected. This delay is provided by the DP tube circuit.

To assure obtaining a closure of adequate length, the L relay is operated from the P relay, and the L relay when operated will remain operated for a timed period due to the action of the capacitor in its secondary winding circuit. A capacitor timed relay is used as the RAA relay to assure holding on very slow pulsing.

L2-2.1.4.1 DC and AC Power Supply

Two ungrounded sources of dc power, in addition to ac for the heaters of the vacuum tubes, are required for the circuits mentioned above. An ungrounded source of dc power is required because of the operation of the amplifier circuit at a potential above ground determined by the conditions in the sender circuit. The second ungrounded dc supply

supplements the +130 volt office battery potential. The amplifier is sensitive to small changes in dc voltage; hence, it is necessary to regulate the rectified ac supplied to it which may vary from the nominal value by ± 10 percent. A connection is made from the ac supply to the transformer tap corresponding to the nominal supply voltage.

The R electron tube rectifies the high voltage ac from the B transformer, and a filter (R1 retard coil and R11 and R12 capacitors) reduces the ripple in the dc voltage supply to the PA and DP electron tubes. The dc voltage at the output of the filter fluctuates as the RMS value of the ac supply voltage fluctuates. The VR2 and VR3 gas filled voltage regulator tubes and a 10,000-ohm resistor are connected in series across the dc supply at the output of the filter. The current through the tubes and resistor will vary as the voltage fluctuates. But, the voltage drop across the voltage regulator tubes VR2 and VR3 will remain substantially constant due to the characteristics of the tubes. This property is used for controlling the voltage of other parts of the circuit or as described in a later paragraph. The load current is passed through a circuit consisting of the VR1 electron tube and a 33,000-ohm resistor in parallel.

The grids (elements 3 and 7) of the VR1 tube are connected to terminal 5 of VR2 tube. So long as the VR1 tube operates between saturation and cutoff, voltage changes between grids and cathodes of VR1 tube will be a minimum. For instance, if the rectified dc voltage should go up, the dc potential at the cathodes would tend to go up. Since this would cause the grids to become more negative with respect to their cathodes, the current flowing through the VR1 tube is reduced and a greater proportion of the load current will flow through the VR1 resistance which is in parallel with the VR1 tube. The potential across the load increases and the cathode voltage will therefore tend to remain at approximately the original value.

The P gas filled tube and B fuse are provided in order to prevent a dangerously high voltage from being connected to leads external to this circuit in the event that the high-voltage section, dc or ac, of the amplifier power supply becomes grounded. In operation, the P tube will fire when the voltage to ground exceeds approximately 180-volts. The resulting current through the B fuse will cause it to operate and open the circuit.

Plate supply for the bias control circuit is obtained from the office +130 volt supply. In addition, a booster voltage for plate 4 of the B1 electron tube is obtained from rectified and filtered ac power. Grid bias for grid 3 of B2 electron tube is obtained from the office 48-volt battery through a voltage divider.

The ac power is connected to the primary of the ac transformer through contacts of the ac relay under control of the MAC key. The MAC key when operated also closes a circuit from the break contact of the NVA relay to the alarm circuit. The NVA relay is operated from rectified ac and is held operated as long as ac is connected. The release of the NVA relay, owing to operating the ac fuse or a power failure, will therefore operate the alarm. The control circuit for the start monitor relay in the AMRST control circuit is closed through a make-contact on the NVA relay. Releasing the NVA relay will therefore prevent monitoring operations from starting or continuing if in operation at the time of release.

L2-2.1.4.2 Outgoing Sender Connection

Dial pulsing out of a OS is done in one of three ways:

- (a) Slow-speed loop pulsing.
- (b) High-speed loop pulsing.
- (c) Battery and ground pulsing.

The connection to the monitor amplifier and the amplifier condition is the same for all three pulsing conditions. The connection of the two control leads to the amplifier are made across the tip and ring leads on the trunk side of the pulsing contact or contacts in the sender. An ungrounded amplifier is required in this case in order to eliminate earth potential effects on the amplifier operation. The potential existing across the tip and ring will vary during pulsing from zero or a positive voltage (ie, potential on the ring less negative than the tip potential) with the loop closed, to full battery voltage when the loop is opened. The battery voltage is that existing in the distant office. Since the rate of change in voltage is reduced by the capacity between trunk conductors and to ground, the voltage across the tip and ring at the OS may not reach full battery potential during an open period. The biasing voltage for the amplifier is therefore kept low, approximately 15-volts. This bias voltage is obtained from a potential divider across the VR3 voltage regulator tube. The connection to the OS is established by operating the DSM relay from the AMRST control circuit which connects the T lead from the OS to the biasing circuit and the R lead from the OS to the control grid of the amplifier. The operation of the amplifier circuit during pulsing is described in L2-2.1.4.

L2-2.1.4.3 Dial Pulse Counting (SFD-L233)

During pulsing the pulses are received by the dial pulse amplifier and repeated by the P relay of that circuit to the dial pulse counter consisting of the P- relays. The operation of the amplifier is described in Dial Pulse Amplifier and Repeater, L2-2.1.4.

When the DOS1 relay is operated, AON (SFD-L211) operates and furnishes off-normal ground to bias the L relay over its secondary winding to its back contact and ground through this back contact operates the LA relay. Relay AON also biases RAA to its back contact. When LA operates, it operates LA1 which closes the back contacts of LA to the RAA relay and its associated capacitor. Closure of this path is delayed until LA operates to prevent RAA from operating prematurely when AON first operates. If RAA operated, it would be held operated for approximately 0.1 second by the RA capacitor, thus causing trouble if the AMRST was seized quickly. The RAA armature is controlled from LA1 to prevent interference with the adjustment of the LC relay if RAA lies on its front contact when its biasing winding is open.

When the AMRST is seized, DON (SFD-L211) operates from DOS2. Relay DON closes leads to permit control of the steering circuit of the register. Relay DON also closes the control leads for the PST relay and connects ground to start monitor timing. The operation of the AS and ASA relays associates the A digit register relays with the output of the dial pulse counter (SFD-L236). The circuit now awaits pulsing.

The L relay follows pulses received from the P relay through its primary winding and transmits them through the CDP relay to the LC, LD, and LE relays. When L operates, it releases LA which closes a circuit to operate the RAA relay on its secondary winding and discharge the RA capacitor. When LA reoperates as L releases at the end of a pulse, the RA capacitor will charge through the RAA relay holding it operated until the charging current decreases to the point where the bias current in the primary winding releases the relay. The circuit elements in the bias and charging circuit paths have been so chosen that the RAA relay will just hold over the longest open between pulses. It is held to close time tolerances since, when it releases, the digit just pulsed must be registered and the circuit prepared to receive the next digit.

Relay RAA operating at the start of the first digit operates PST which locks to DON. Relay PST prepares a path for operating RA1 (SFD-L236) at the end of the digit, recycles the timer and operates PH. Relay PH closes circuits used in registering the digit and advancing the steering circuit at the completion of a digit.

In order that the L relay will produce usable pulses at its contacts even though line conditions and central office voltage have wide variations, certain corrective devices have been added to the L relay and its associated circuit. These are described in the following paragraphs.

The L relay has no retractile spring but instead is provided with a tertiary winding energized in the direction to hold contact 5 closed, whereas the primary winding is energized in the direction to hold contact 4 closed. This partly compensates for battery voltage variations, and also causes the relay to release quickly when the primary winding is opened, since the releasing force does not decrease as the armature restores to normal as it would if a retractile spring were used.

The secondary winding and its associated circuit is provided in order to insure that the contact closure will not be less than a minimum time determined by the time constant of the secondary circuit. When the contact 5 closes, capacitor LA1 charges in series with the secondary winding. The charging current is in the direction to hold the relay released, and the relay will be held released, at least until the capacitor becomes sufficiently charged and the current reduced so that the magnetizing force of the secondary winding becomes less than that of the primary winding. When contact 5 opens, capacitor LA1 discharges in series with the secondary winding and the LA1 resistor. The direction of the current is such that the armature is held against its contact 4, at least for the time required for the capacitor to discharge and reduce the current sufficiently so that the secondary magnetizing force plus the tertiary magnetizing force becomes less than the primary magnetizing force. The secondary winding, therefore, causes the L relay to stay on whichever contact has closed, for a time long enough to perform the required functions, even though the contact closures of the P relay are short.

The LC, LD, and LE relays follow the front contact pulsing of the L relay and convert a closure and open of the L relay contacts into a single pulse to the counting relays. At the completion of a pulse cycle (which consists of a closure and open of the L relay front contacts), these relays transmit a pulse to one or two leads, used alternately to operate the P1_ to P6 counting relays. Relay LC operates when L operates on the first pulse, and the LE operates by its primary winding in series with the LC when L releases on the open following this pulse to remove the shunt from the LE winding. The operating ground for LE is supplied from front contacts of RAA. Relay LE operating closes a ground to one of the two operating leads for the pulse counting relays. When L operates on the second pulse, LD operates on its primary winding in series with the secondary winding of LE. This holds LE since its original operating path is opened and LC is released by LD. When L releases at the end of the pulse, LD and LE release. Relay LE removes ground from one of the counting relay operating leads and supplies it to the other. Any possibility of LD releasing before LC and thereby preventing the release of LC and LE is prevented by locking the secondary winding of LD to a front contact of LC. If more digits are received, this cycle will be repeated every two pulses of the digit. Upon the completion of a digit, the release of RAA will release LC and LE if they have been left operated by the reception of an odd number of pulses.

The pulses of each digit are counted on relays P1 to P6 which operate in rotation from alternate contact closures of LE. In general, each relay releases the previous relay except that P6, if operated, remains operated to indicate that a digit of more than five pulses has been received. At the completion of a digit the count is first transferred to the register relays over two out of five leads and then the operated counting relays are released in preparation for the next digit. Relay P6A is an auxiliary relay to the P6. The relays operated after each pulse are as follows:

<u>Pulse No.</u>	<u>Relays Operated</u>
1 LC, LE	P1
2	P2
3 LC, LE	P3
4	P4
5 LC, LE	P5
6	P5, P6, P6A
7 LC, LE	P1, P6, P6A
8	P2, P6, P6A
9 LC, LE	P3, P6, P6A
10	P4, P6, P6A

The first operation of LE operates P1 on its primary winding through break contacts of P2, P3, P4, and P5. The P1 locks to other break contacts of P2, P3, P4, P5 and RA1. The second pulse, through break contacts of LE and make of P1, operates P2 which releases P1 and locks itself through the same path which previously locked P1. The third pulse, through back contacts of P4 and make of P2, operates P3 which unlocks P2 and locks itself. This action continues until the sixth pulse operates P6 through make contacts of P5. Relay P6 operates P6A and locks for the remainder of the digit but does not unlock P5. Relay P1 operates and locks again on the seventh pulse, this time, through make contacts of P6 and releases P5. The eighth, ninth, and tenth pulses operate P2, P3, and P4 respectively, each relay as it operates unlocking the one ahead of it.

When the RAA relay releases upon completion of a digit, certain of the P relays will be locked to RA1. The break contact of RAA closes ground to two leads which are steered by the operated P1 to P5 relay and the P6A to the proper 2-out-of-5 leads to operate register relays. The release of the P- relays and the control of steering circuit by the PH and RA1 relays is described in a subsequent paragraph.

L2-2.1.4.4 Digit Registration and Steering (SFD-L234-37)

Five register relays and two steering relays are provided to accomplish the registration of each digit received from the pulse counting relays.

When the AMRST was seized, ground through the ONR operates the AS, ASA, and MK relays (SFD-L235). Relay ASA connects the A(0,1,2,4,7) relays to the output of the pulse counting relays (SFD-L236). Relay MK is slow operate to permit AS to operate and lock through back contacts of BS to ONR before the operating path is broken by MK. Relay ONR provides general off-normal grounds. The circuit now awaits the first digit.

As previously described, a circuit through the counting relays will operate two of the A(0,1,2,4,7) relays at the end of the A digit (SFD-L236). Assuming, for discussion, a number other than 0, 1, 8, or 9 is dialed. The two operated relays will lock to ONR. The locking path for A0 or A1 is through make contacts of one of the other three operated relays. Relay RA1 operating at the end of a digit closes ground from make contacts of one of the other three operated relays). Relay RA1 operating at the end of a digit also closes ground from make contacts of the PH relay through AS and A2, A4, or A7 operated to operate BS and BSA. Continuity contacts on RA1 also open the operating path of PH and close a locking path through break contacts of T0. The continuity 1, 2, 3T on BS insures locking BS before its operating path is opened, the operating path being opened to prevent the locking ground from backing into the operating circuit. The 1, 2, 3B continuity opens the path by which AS and ASA were locked to off-normal ground and connects these relays to ground through the T0 relay and its T0 register shunt. Relay T0 operates and opens the holding path for the PH and P- relays. Relay T0 locks until RA1 releases at the start of the next digit. Relay PH in releasing releases AS and ASA, and opens the register relay operating grounds. Relay ASA in releasing transfers the counting relay output leads from the A digit register relays to the B digit register relays. The circuit now awaits the B digit. Succeeding register and steering relays are operated as just described.

L2-2.1.5 Multifrequency Pulse Amplifier and Repeater

This circuit is arranged for completing a transmission circuit for the MF pulses of a sender to the receiver used with the AMRST circuit.

L2-2.1.5.1 Testing Multifrequency Outgoing Senders

The MFS relay is operated from the MOS2 relay when the multifrequency pulse repeating circuit is to be connected to an OS (SFD-L208). The MFS operated connects the T and R leads from the sender to the MF2 repeating coil. It also connects the output of the MF1 transformer after attenuation by the MF pad to the AMRST MF receiver (SFD-L232). The output of the MF2 repeating coil is connected through the MF3 capacitor to the grids of the MF electron tube. The combination of the MF3 capacitor and MF4 grid resistor correct for a slight change in transmission loss in other parts of the circuit over the 700- to 1700-cycle frequency band. Current flowing from the +130 volt office battery through the primary windings of the MF1 transformer, the plate to cathode circuit of the vacuum tube to ground through the MF1 resistor produces a voltage drop across the MF1 resistor. This voltage drop is impressed across the grid-cathode circuit and serves to automatically adjust the plate current. The value that will be reached is dependent upon the characteristics of the tube used. The MF1 capacitor is shunted across the MF1 resistor in order to maintain the grid bias at a constant average value when a modulating ac voltage is impressed on the grid during pulsing. A fraction of the ac voltage at the plates of the MF tube is

fed back to the grid through the voltage divider circuit which consists of the MF2 capacitor and MF2 and MF3 resistors. Feeding back a portion of the ac voltage from the plates to the grids effectively reduces the change in voltage that an ac input signal will produce at the grids. This reduces the effective gain of the tube.

L2-2.1.5.2 Receipt of Multifrequency Pulses

The frequencies comprising a digit pass through the MF amplifier into the receiving circuit. Relay MFS, which operated from MOS2, operates MFN. Relay MFN connects off-normal batteries to the multifrequency receiving circuit. Relay MFN connects ground and battery to the primary winding of PT0 in a direction to operate this relay (SFD-L234). However, a ground on the M lead from the multifrequency receiver is connected to the secondary winding of PT0 in the nonoperate direction. Since the secondary winding is the more powerful, PT0 is held on its back contact. The operation of the multifrequency amplifier is covered in Multifrequency Pulse Amplifier and Repeater.

Each signal sent to the AMRST from the OS consists of 2-out-of-5 audio frequencies designated 0, 1, 2, 4, and 7 (SFD-L231). The entire code used is as follows (note that the two numerical frequencies may be added to obtain the corresponding digit for digits 1 through 9):

<u>Digit</u>	<u>Frequencies</u>
0	4, 7
1	0, 1
2	0, 2
3	1, 2
4	0, 4
5	1, 4
6	2, 4
7	0, 7
8	1, 7
9	2, 7
KP	2, 10
AT	7, 10

Actual frequencies are as follows:

<u>Frequency Designations</u>	<u>Cycles per Seconds</u>
0	700
1	900
2	1100
4	1300
7	1500
10	1700

L2-2.1.5.3 Steering and Registration (SFD-234-37)

When a signal is received, the receiver grounds the J lead to the AMRST (SFD-L234). This is returned through back contacts of the T0 relay to the L lead where it closes the operating circuit for the receiver channel relays 0, 1, 2, 4, and 7. With the AS and ASA relays operated, grounds from the operated channel relays will operate the corresponding A(0,1,2,4,7) relays. At this same time, the receiver grounds the H lead which operates the BS and BSA relays. A continuity of BS opens the locking path of AS and connects it in series with the T0 resistor to the H lead to the receiver. At the time the H lead is grounded, the receiver removes ground from the M lead permitting the PT1 capacitor to start charging in series with the secondary winding of PTO. Relay PTO holds operated until the charging current and the secondary ampere turns are reduced to the point where the primary winding can operate the relay. When PTO operates, it connects the T0 relay in multiple with the T0 resistor and T0 operates. The timed delay provided by PTO and its associated capacitor insures that the register relays operate before T0 operates to start release of the channel relays. The T0 opens the L lead to the receiver and locks to the J lead. The channel relays of the receiver release causing ground to be removed from the H and J leads and connected to the M lead from the receiver. Relay AS, ASA, and T0 release, PTO operates and the circuit is ready for the next digit.

SECTION L, PART 3

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L3 CHECKING, TEST COMPLETION AND RELEASE

Part L3 describes how the Automatic Monitor Register Sender Test (AMRST) checks the performance of the registers and senders under test. For simplicity the description is separated into Originating Register (OR), Incoming Register (IR), and Outgoing Sender (OS) tests.

L3-1 ORIGINATING REGISTER (OR) TEST

When the OR recognizes pulsing is completed, it seizes a Completing Marker (CM) through the ORMC. The CM, recognizing it is handling a Monitor (MON) test call, stops its regular progress and seizes the MTFC which connects to the AMRST. The digits stored in the OR, along with other information, are passed through the ORMC, CM, and MTFC to the AMRST where they are checked against the digits that were registered at the start of the test in the monitor by the master test control. If the digits match the test has been completed satisfactorily and an OK signal is indicated. This starts release of the OR. Operation of the RL key in the MTC starts the release of the AMRST, however the monitor and the OR will not fully release until the STT key in the monitor has been released.

L3-1.1 PULSE END AND CONNECTION TO MARKER

When the OR recognizes that pulsing is completed, it connects to a CM through the ORMC. At the same time, the AMRST connects to the marker through the Master Test Frame Connector (MTFC) to obtain the information transmitted from register to marker.

When the ORMC connects the register to a marker, a circuit is established from relay MT through break contacts of MTR and make contacts of RPE2 and DOR2 to the MON lead to the OR and thence to operate the MON relay in the marker to prepare it for a monitored call (SFD-L318). The MT relay operates in series with the MON relay of the marker. The MON relay locks to MT on the MONL lead from CM to AMRST. Relay MT grounds the STG lead to the MTC circuit to prevent the call from being abandoned during the period when the marker is on the connection (SFD-L109).

The MON relay of the marker prepares the marker for operation with the AMRST and also serves to close through a number of direct leads from the monitor to the marker. Ground from the AMRST on the MON1 lead operates the MON1 relay of the marker (SFD-L309). Relay MON1 opens the normal internal release paths of the marker and also prevents it from starting a trouble record. Ground from the monitor DOR1 relay on the RTST lead operates the RTST relay of the marker (SFD-L309). Relay RTST stops the regular progress of the marker and closes the DIS, RLT, and RBT leads to the AMRST (SFD-L319). These leads give the monitor control of the release of the marker. For OR testing, the CM is used only to obtain the information passed from register to marker.

When RPE2 of the AMRST operates, as previously described, it connects battery to the TRST lead to operate the monitor preference relay MON in the MTFC which in turn operates the CI relay (SFD-L309). Relay CI opens the operating path of the monitor TRB relay and closes ground to the ON lead to operate off-normal relay ON in the MTFC. Relay CI operates C11 (SFD-L117) which operates the MCA, MCB, MCD, and MCQ relays in the AMRST which connect groups of leads from the AMRST to the MTFC. Relay MTR1 operates through CI to open the TRB lead. Relay CI also connects ground to the MKB lead to the marker. This lead is multiplied to all markers but is effective only in the marker with an operated MON relay where it is extended to operate the multicontact relays MKB- in the MTFC which connects that marker to the MTFC for testing operation. The AMRST is now connected to the CM through the MTFC and registers information necessary for test purposes.

L3-1.2 REGISTRATION OF INFORMATION FROM MARKER

The physical location of the calling line as stored in the OR is passed to the AMRST through the MCA relay. If the NTC key at the MTC is not used it will be the location of the Originating Test Line (OTL) (SFD-L310).

The number of the marker handling the call is recorded through the MCA relay. The units number is recorded on one of the MO-9 relays and, if there are more than 10 markers, the tens number is recorded on the MKT0 and MKT1 relay (SFD-L310).

Class indications passed from OR to CM are recorded through the MCD relay. These indicate the reaction of the register to the test applied to it. The specific use of each indication is covered in detail as the tests are described (SFD-L311).

The OR grounds the LT lead and the D or MF lead and the OR lead to the CM where they are extended to the AMRST to operate one of the corresponding relays through the MCA and MCQ relays (SFD-L311). In the check path, these relays are matched against the pulsing instructions set on the keys or switches of the MTC. The specific use of each indication is covered in detail as the tests are described.

The called number information passed from OR to CM is closed through the MCB relay. Five leads for each of eleven digits, and an M7 lead to register a 7 beyond the last digit is provided. Relays KAL(2/5) operate in each digit position to correspond to the information passed from register to marker (SFD-L316). The operated relays lock and control the number checking path in combination with the OR relays operated from keys or switches of the MTC circuit at the start of the test.

L3-1.3 RELEASE OF MARKER AND MASTER TEST FRAME CONNECTOR

The TRT tube and associated relays comprise a timing circuit which determines how long the CM will be held. Relay TRT1 operates through make contacts of MT, RPE2, and CI to start the timing (SFD-L320). Thus, timing is started as soon as both the marker and the MTFC have been seized. Considering for the moment, operation with ORH unoperated, the TRT timing interval of 165 to 245 milliseconds is just sufficient to permit operation of the cut-in relays at the marker and AMRST ends of the MTFC and also operation of the monitor relays which record the information received from the marker.

Operation of the TRT1 relay connects ground to the RLT lead to the marker. This ground is extended through the marker and marker connector to operate the RL relay of the OR (SFD-L319). Relay RL releases the OTL from the register. Relay TRT1 also closes the charging circuit for the TRT capacitor which charges in series with the TRT relay and the TRT3 resistor. When the TRT capacitor charges to approximately 70-volts, the TRT tube ionizes across its control gap 1 to 4. With the tube ionized, current flows in the main 12 gap to operate the TRT relay. The TRT operates the MKR relay which locks (SFD-L320). Relay MKR connects ground to the DIS lead to the marker operating the DIS1,2 relays which operate the MRL relay of the OR. This releases the ORMC and the CM.

If the MTFC is busy at the time the AMRST starts to select it, the monitor will wait until it becomes idle. The CM will be held during this period. If the MTFC is busy for a long interval, a 2.25-second timer in the marker will function to release the marker and sound an alarm. When the CM releases itself, MT will release and open the circuit to MKR. The trouble lamp will light, and the MST lamp will remain lighted as an indication that the marker phase of the call was not completed satisfactorily. If the OR does not reach the marker, the test will end similarly but there will be no marker alarm.

To test whether the marker connector furnishes a holding ground for the SR relay of the register, the ORH key is operated. This operates the ORH relay (SFD-L320) which changes the marker holding time to 665 to 1060 milliseconds. (The RBT release should not be used with this test.) When the TRT1 operates, the RL of the OR operates to remove the tip and ring holding path of the L and SR relays of the register. If the ORMC holding path for the SR relay is open, SR will release removing ground from the H lead to the AMRST (SFD-L208). This will cause TAC to release and TAC2 to operate. Under this condition a path is closed from ground on a break contact of MKR through make contacts of ORH, RPE2, TAC2, and ONT1 and break contacts of OK to operate TBL (SFD-L326). As an indication that this test has failed, the ORH lamp will light (SFD-L322). This lamp is lighted only if all prior tests are satisfactory. The circuit of the lamp is opened at CKE so that the lamp will not light in case of a failure to check the numbers.

In addition to releasing the CM and OR as just described, the MKR relay also operates the RTC1 relay (SFD-L117). Relay RTC1 locks and opens the TRST lead to release the AMRST preference relay MON in the MTFC. MON then releases CI which removes ground from the ON lead to the master test frame connector to complete its release. Relay CI removes ground from the MKB lead to the marker to release the cut-in relays at the marker end of the MTFC if the release of the marker has not already progressed to the point of releasing these relays. Relay CI releases C11 which releases MCA, MCB, and MCD at the AMRST end of the connection to the marker. When the MTFC completes its release, MTR1 is released. Relay RTC1 and MTR1 remove ground from the MON1 lead to the marker, but this action is not required for register testing since the marker is already releasing.

Relay RTC1 also operates RTC2 which closes a path to the winding of the CKS relay.

L3-1.4 NUMBER CHECKING

If all the tests imposed on the OR are completed satisfactorily, a ground is connected to operate CKS through a contact of RTC2 (SFD-L322). The circuit details of the check path are covered in the descriptions of the individual tests in paragraphs which follow.

When CKS operates, it locks and lights the CKS progress lamp to indicate that the number is being checked. Relay CKS also extinguishes the previously lighted MST1 and ORON progress lamps.

The CKS also connects resistance battery to operate CKN if the numbers registered check (SFD-L324). When DOR2 operated from the start key of the MTFC it operated the RTC relay which connected five leads for each code or switch of the master test control to the digit register relays (SFD-116). For instance, the A0, A1, A2, A4, and A7 leads are connected respectively to the A0, A1, A2, A4, and A7 relay in the AMRST. The number set up on the keys or switches, which was the number pulsed into the OR, operates the register relays on a 2-out-of-5 basis. Each of these relays is paired with a corresponding relay which records the number passed from register to marker. For instance A0, A1, A2, A4, and A7 are paired respectively with KA0, KA1, KA2, KA4, and KA7 (SFD-L324). The check path is wired through the make contacts of the pair in series. Hence, completion of the check path requires that the two numbers be exactly the same. At the time the CKS closed battery to the check path, it also closed the operating path for CKE (SFD-L325). Relay CKE is slow-operate to permit the CKN to operate if the check path is complete. When CKE operates, ground is connected through break contacts of CKN to operate TRR1 and cause a trouble record to be made, or through make contacts of CKN to operate OK.

L3-1.5 TROUBLE RECORD (SFD-L325)

When TRR1 operates, it locks and operates TRR2. Relay TRR2 opens the OK operating path to prevent a late number check from operating the OK relay. The MKB lead is opened by TRR1 to prevent operating marker cut-in relays.

Relay TRR1 closes battery to the TRST lead to operate the monitor preference relay MON in the MTFC (SFD-L309). When the AMRST gains access to the MTFC, CI operates. Relay CI closes ground to the ON lead to operate off-normal relays in the master test frame connector and another ground from make contacts of TRR1 to the STR lead. The STR lead ground is extended through the MTFC to the trouble recorder control circuit which prepares the trouble recorder and MTFC to receive a trouble record. The CI also operates the CII relay which operates MCA, MCB, MCD, and MCE relays.

The primary objective of this trouble record is to utilize the facilities of the trouble card to indicate the pulsing performance of the OR. The KAL(2/5) relays previously operated to record the called number passed from register to marker extend their locking grounds into the MTFC through the MCB relay (SFD-L316). Similarly the called number registered by the AMRST from the MTC circuit is extended through the MCE relay to the master test frame connector (SFD-L116). The LT lead is used to indicate the translator lead grounded to the CM by the OR.

Additional information is also included in the trouble record. The MOR lead to the MTFC is grounded through DOR1 and MCA to indicate that the trouble record is being made by the AMRST on an originating register test call (SFD-L326). The SRT lead through STT and MCA indicates that it is a test call. The originating test line location and the marker number is recorded through the MCA relay (SFD-L310). Relay MCA connects ground to the RG, CN, and FR leads to the OR where they are extended through the M relay to leads to the MTFC which identify the register (SFD-L326). The RG, FR, and CN leads are used respectively to indicate the position of the register in its marker connector, the frame on which the marker connector is located, and the position of the marker connector on that frame. The information recorded through the MCD relay is also included in the trouble record. This information indicates register response to certain tests imposed on it.

After a trouble card has been perforated in accordance with information conveyed by grounded leads extending from the AMRST to the trouble recorder through the MTFC, ground is connected to the TRC lead to operate the TRC relay which locks (SFD-L326). Relay TRC opens the TRST lead to release the master test frame connector, trouble recorder, and the CI, CII, MCA, MCB, MCD, MCE, and MTR1 relays of the monitor. Relay TRC also operates TBL.

L3-1.6 TEST COMPLETION (SFD-L325)

When CKN operated, as an indication that the number check was satisfactorily completed, it connected ground to a contact of TAC2. When TAC2 operates as a sign that the OR has started to release, the ground operates the OK relay which locks under control of TAC2. Relay OK lights the OK lamp and extinguishes the CKS lamp. Relay OK operates the TA relay to stop timing of the test. Relay OK opens the operating circuit of TBL.

When an abandoned call test is made and if the register releases satisfactorily, TAC2 will operate and close a ground to operate the OK relay. If the register fails to release and selects the marker, the operating path for OK just described will be opened at RPE2, and the test will fail because the operating path for CKS will be open.

If the OR fails to perform satisfactorily during the tests, the TBL relay will operate (SFD-326). Relay TBL locks and lights the TBL lamp. Relay TBL opens the operating path of the CKS relay to prevent a number check from starting if the originating register hold test fails. Relay TBL operates the TA relay to stop timing of the test. Relay TBL also opens the operating path of OK.

Relay TBL may operate as a result of a number check failure, in which case it operates from TRC as described previously. If the register timing of the first two party test is excessive or the digit timing test fails, a positive indication of trouble is obtained, and TBL is operated directly. In other cases, the only indication of trouble will be that the operating path of the CKS relay will be open. Under this condition, the TM timer will function to operate the TBL relay.

An exception to the immediate operation of the TBL relay from a timeout occurs if it is desired to obtain a trouble record to check on class information passed from OR to CM. This information for various tests is conveyed on one or more of the PD, PK, PS, SCK, TP, and RP leads. If the test call reaches the point of selecting a marker, CTT operates opening the normal operating path for TBL following a timeout. Relay CTT also closes a ground through a make contact of RTC2 relay. This ground operates TRR1 and a trouble record is made as described in Trouble Record (L3-1.5). If the maintenance employee does not wish to wait 40 to 70 seconds for the timeout, the QTR key may be operated when the CKS lamp does not light following marker release. Operation of QTR will operate TRR1 if CTT and RTC2 are operated.

When the OK relay operates, it removes the 10-ohm ground from the winding of the TAC relay. This permits the ON1 relay of the OR to release and start complete release of the register. The M and MB relays of the OR will, however, be held operated until the AMRST is released. If TBL operates, the ON1 relay of the register will not be released, thus permitting inspection of the OR while in its off-normal condition.

L3-1.7 RELEASE

The operation of the RL key of the MTC circuit operates the KR relay which removes ground from the STG lead, releasing the DOR2 relay (SFD-L109). Relay DOR2 opens all leads to the register, permitting its release. Relay DOR2 also releases ONT1 and ONT2. Release of these three relays cause the release of all operated relays associated with the particular call. The DOR1 and relays operated from it will remain operated until the OR key of MTC control circuit or the STT key of the AMRST is restored to normal. Relay TSR releasing from ONT1 recloses battery to the N lead to the master test control circuit to permit another call to be started. Relay TSR is slow-release to permit all relays of the AMRST to release before permitting reseizure.

L3-1.8 REPEAT TESTS

Operation of the REP key of the MTC circuit causes repeat tests to be made. The call progresses as previously described for an OK call up through the point of operating the OK relay. The OK relay closes ground to the REP lead to the master test control circuit to shunt down its N1 relay which removes ground from the STG lead to release the AMRST. When TSR releases and closes battery to the N lead, the master test control circuit proceeds to initiate another test call. If a trouble is encountered, TBL will operate to sound an alarm from battery received on the AL lead from the REP key of the MTC circuit, and no further tests are made.

L3-1.9 INDIVIDUAL LINES

A regular test call simulating an individual line is made by the AMRST. The call progresses as described in the preceding paragraphs. A ground from ORST operated, the normal CN key, the operated FD2 relay, the normal 2P relay, RBT key, ORAB, RPS, and RPD relays to the operated PK relay where it is extended to the operated MST relay to operate CKS directly if the register has performed satisfactorily.

In the event of a failure to check, no ground will be applied to CKS and the timing circuit will time out to indicate a circuit failure. The MST lamp being out indicates that the marker functions were completed and, if the CKS lamp does not light and lamps MST1 and ORON remain lighted, a failure of information other than the number recorded from the register to match that of the test circuit is indicated. The relays operated by the register on the test will be indicated on the trouble record card. This card will be perforated following a time out or, if it is apparent that the test is failing, the QTR key will bring the trouble card immediately.

L3-1.10 PARTIAL DIAL

For a partial dial test, the code digits are set on the digit keys or switches at the MTC circuit. For noncoin calls the number of digits used is variable. The minimum number being one digit, set on the A key or switch, and the maximum number being one less than required for a normal call. Also, the RPD key must be operated. When dial pulsing, the most accurate check of the register timing interval will be obtained with a low number, preferably 2, as the A digit, and using the 15 pps minimum interrupter. For TOUCH-TONE tests, any digit may be used as the A digit. A check of the recycle feature of the register, TM, timer is made with more than one code digit set on the digit keys or switches. The numbers should be high, and for dial pulsing use the 7 pps minimum interrupter. If the TM timer does not completely recycle for each digit, there will be an appreciable reduction in the register partial dial timing interval, nominally 25 seconds.

The RPD relay is operated from ground through ORST and the RPD key (SFD-L219). The test circuit will function normally until the A digit is pulsed and the OSA relay released. The OSB1 relay will then operate to light the OBS lamp and cause operation of the RPD relay. The OR is then allowed to time out and this will result in operation of the marker start relays MST and MST1 of both the register and monitor. With the RPD relay operated, the PD relay must be operated from the register for the circuit to check.

For timing test, the period between the operation of the OSA lamp and the MST1 lamp should be measured. This interval should be 21 seconds minimum, 30 seconds maximum with the register OVL relay normal or 4.8 seconds minimum, 7 seconds maximum with the OVL relay operated.

L3-1.11 PERMANENT SIGNAL

For a test of the permanent signal feature of the OR, the RPS key should be operated to operate the RPS relay (SFD-L209), but no code or numerical digit keys or switches should be operated. When the start key is operated, the register is seized in the usual manner, resulting in operation of the ORON relay which lights the ORON lamp and operates relay FD2. No digits will be dialed, and the register will time out to cause operation of the marker start relays MST and MST1 of the OR and AMRST. With the RPS relay operated, the PS relay must be operated from the register for the circuit to check.

For timing test, the period between the operation of the OSB lamp and the MST1 lamp should be measured. This interval should be 21 seconds minimum, 30 seconds maximum with the register OVL relay normal or 4.8 seconds minimum, 7 seconds maximum with the OVL relay operated.

L3-1.12 PRETRANSLATING

When the office codes from an area are so complex that it is not feasible for the OR to determine from its own cross-connections the number of digits to be received for each code, a feature will be provided to summon the pretranslator after the second or third digit is recorded. The pretranslator will then inform the OR how many digits are expected. This feature of the register is checked on regular calls by the end result achieved. The particular code and number of digits set on the code and numerical keys or switches must match the position of the station delay timer key STD. If the code and number of digits are such that no station delay is expected, the key must be normal, and if the code and number of digits are such that a delay is expected, the key must be operated. No check is made of the OR operation with the pretranslator.

L3-1.13 ABANDONED CALLS

To check the ability of the OR to release if the call is abandoned, the A digit key or switch should be operated at the MTC circuit along with the RAB key. A digit 2 through 8 should be used. The AMRST will function as on a regular call until the A digit is pulsed and the OSB1 relay operated. Relay OSB1 will operate ORAB which opens the ring conductor to cause release of the register. A ground will be extended through the operated ORAB relay to a break contact of RPE2 where the release of the register is checked.

L3-1.14 BUSY TONE TEST

If the CM is unable to complete a call from an OR in the usual manner, it will operate the register BT relay causing the register to return a busy tone to the customer. This feature is tested by operating the RBT key in addition to the regular keys. The RBT key operates the RBT relay. After the timed TRT interval, the MKR relay operates and the AMRST grounds the RBT lead to the marker operating its RBT relay. This will cause the register BT relay to be operated in place of the MRL relay. The BT relay of the AMRST will also be operated. The OR is then allowed to time out to release and, during the time out period, busy tone can be heard at the receiver if the MOTL key is operated. When the register timing interval is completed, the register RL relay operates to release the register SR relay which allows the TAC2 relay of the AMRST to operate to close the path to relay OK. The timing interval can be measured by the time of application of the busy tone and the interval should be 21 second minimum to 30 seconds maximum.

L3-1.15 TWO-PARTY LINES

The OR, when seized by the Dial Tone Marker (DTM) and given a two-party class, operates its TPA relay which connects the tip and ring conductors to it's TP relay for an interval of 210 to 330 milliseconds as timed by a tube timer. If the line is a tip party line, a resistance ground will be connected to the tip to cause operation of the register TP relay. When the timed interval has elapsed, the ring is connected to the OR L relay and the tip connected to ground through the dial tone repeating coil winding. This causes operation of the L relay followed by the SR and ON1 relays in the register. The operation of the ON1 relay completes the circuit which supplies dial tone to the calling customer. After the OR records the last digit but before connecting to a CM, the register disconnects the L relay and reconnects both the tip and ring conductors to the TP relay for a second timed interval. On service calls, the results of both the first and second tests must agree or the marker will block. The test circuit is arranged to check the operation of the register TP relay on each of these tests by providing match tests under some conditions and mismatch tests under other conditions.

L3-1.15.1 Two-Party Tests (SFD-L224)

For these tests, the 2P key and one of the keys RTP, RRP, TPF, or RPF are operated (SFD-L209).

Key RTP applies an operate test through the TPK resistance ground to the register TP relay on both the first and second tests.

Key RRP applies a nonoperate test through the TPK- resistance ground to the register TP relay on both the first and second tests.

Key TPF tip party first failure applies the operate test to the TP relay on the first test and the nonoperate test to the TP relay on the second test.

Key RPF ring party first failure applies the nonoperate test to the TP relay on the first test and the operate test to the TP relay on the second test.

When the start key at the MTC circuit is operated resulting in operation of the DOR2 relay and the ORST relay, the 2P relay operates preparing the test circuit for the two-party line test by connecting the TPK relay to the ring conductor.

The OR is seized under control of the MTC circuit and the marker. When the tip and ring leads are cut through to the AMRST, the TPK relay operates over its secondary winding. The TPK relay is connected to the ring conductor to check that the register is connected at the start of this test. Relay TPK1 operates (SFD-L209) from TPK and connects the R lead from the register to the dialing circuit or TOUCH-TONE signaling circuit. This provides a loop for operating the register line relay when the register completes the two-party test.

If the T and R leads are not connected together at the OR, it is not possible for the register to record a tip party indication and a test failure will result if either of the keys RTP or TPF are used. The test will proceed to the point of checking the class marks and will block because of the absence of the TP indication.

When the register SR relay operates, it operates the TAC and TAC1 relays of the AMRST; this causes operation of the ORON relay. Relay FPT operates from ORON signifying the elimination of the first party test and closes ground to cause pulsing to start. The tip party line conditions are removed by operation of the SY relay or the SPB relay.

The maximum interval of application of the register TP relay to the line is measured by the sum of the release times of the TPT and TPT1 relays. When TPK1 operates, the circuit to the TPT is opened. If both relays TPT and TPT1 release, indicating that the maximum time has been exceeded, the test blocks. The operation of the FPT relay reapplies the operate current to the TPT relay.

When the code and numerical digits set on the keys or switches of the MTC circuit are pulsed, the FD1 and FD2 relays are operated. The SY and SPB relays are normal and, with the FD2 relay operated, the two-party line condition for the second party test is connected to the R conductor. After the last digit is recorded, the register will function to connect the T and R leads together and connect them to the TP relay to make the second party test after which the register MST relay will be operated to summon the CM.

The ORMST relay, in operating, causes operation of the RPE2 relay followed by the MST in the AMRST. Relay MST closes the circuit for operating the SPT relay indicating completion of the second party test (SFD-L209). The register will ground either the TP or RP lead (or both in case the first and second party tests disagree) and this information is received at the AMRST to cause operation of relays corresponding to the lead grounded (SFD-L311). If the information received from the marker matches that set on the keys of the MTC, ground is connected to the check circuit.

If the information does not match, the check ground will not be extended and the test circuit overall timer will function to indicate a failure. In case of a failure to match, the information which the OR passes to the CM and the AMRST can be obtained from the trouble record card. In cases of abandoned, partial dial or permanent signal calls, only the first party test is made and no check is made of the information received by the marker on these calls.

L3-1.15.2 Two-Party Lamps (SFD-L209)

The FPT lamp will be lighted for the period from the start of the test until the first party test is completed. Should the register first party test exceed the time allowed by the release interval of the TPT and TPT1 relays, the FPT lamp will remain lighted. The SPT lamp will be lighted during the time the register makes the second party test.

L3-2 INCOMING REGISTER (IR) TEST

When the IR recognizes pulsing is completed, it seizes a CM through the IRMC. The marker, recognizing it is handling a monitor test call (MON relay operated), stops its regular progress and seizes the MTFC which connects to the AMRST. The digits stored in the IR, along with other information, are passed through the IRMC, CM, and MTFC to the AMRST where they are checked against the digits that were registered at the start of the test in the AMRST by the MTC. If the digits match, the test has been completed satisfactorily and an OK signal is indicated. This starts release of the register. Operation of the RL key in the MTC starts the release of the AMRST, however, the monitor and the register will not fully release until the STT key in the AMRST has been released.

L3-2.1 DISCONNECT (D) TEST (SFD-L308)

When the IR recognizes the end of dial or MF pulsing, it grounds lead D through the winding of a differential relay TC1 and operated MST contacts. Lead D is also connected to the relay D in the AMRST. This is a normal nonoperate condition for relay TC1, but relay D will operate, however. Relay D locks to direct ground on a make contact of relay IRST. This locking ground should operate the IR TC1 relay, causing the register to call in a CM. Relay D also transfers the progress ground from lamp D to a circuit through break contacts of relays CCK and NDK to operate class test trouble relay CTT (SFD-L323). This relay lights the CCK lamp and indicates that the trouble recorder should be called in if the test fails after this point.

L3-2.2 PULSE END AND CONNECTION TO MARKER

When the IR recognizes that pulsing is completed, it connects to a CM through the IRMC. At the same time, the AMRST connects to the marker through the MTFC to obtain the information transmitted from register to marker.

When the IRMC connects the IR to a CM, a circuit is established from MT through break contacts of MTR and make contacts of RPE2 and DIR2 or MIR2 to the MON lead to the register and thence to operate the MON relay in the marker to prepare it for a monitored call (SFD-L318). The MT relay operates in series with the MON relay of the marker. The MON relay locks to MT on the direct MONL lead from marker to AMRST. Relay MT grounds the STG lead to the MTC circuit to prevent the call from being abandoned during the period when the marker is on the connection (SFD-L109).

The MON relay of the CM prepares the marker for operation with the AMRST and also serves to close through a number of direct leads from the monitor to the marker. Ground from the AMRST on the MON1 lead operates the MON1 relay of the marker (SFD-L309). Relay MON1 opens the normal internal release paths of the marker and also prevents it from starting a trouble record. Ground from the monitor DIR1 or MIR1 relay on the RTST lead operates the RTST relay of the marker (SFD-L319). Relay RTST stops the regular progress of the marker and closes the DIS, RLT, and RBT leads to the AMRST. These leads give the monitor control of the release of the marker. For register testing, the marker is used only to obtain the information passed from register to marker.

When RPE2 of the monitor operates, as previously described, it connects battery to the TRST lead to operate the monitor preference relay MON in the MTFC which in turn operates the CI relay (SFD-L309). Relay CI opens the operating path of the monitor TRB relay and closes ground to the ON lead to operate off-normal relay ON in the MTFC. Relay CI operates CII which operates the MCA, MCB, MCG, MCH, and MCQ relays which connect groups of leads from the AMRST to the MTFC. Relay MTR1 operates through CI to open the TRB lead. Relay CI also connects ground to the MKB lead to the marker. This lead is multiplied to all markers but is effective only in the marker with an operated MON relay where it is extended to operate the multicontact relay MKB- in the master test frame connector which connects that marker to the master test frame connector for testing operation. The AMRST is now connected to the marker through the master test frame connector and registers information necessary for test purposes.

L3-2.3 REGISTRATION OF INFORMATION FROM MARKER

The number of the marker handling the call is recorded through the MCA relay. The units number is recorded on one of the relays M0 to M9, and the tens number, if there are more than ten markers, is recorded on the MKT0 or MKT1 relay (SFD-L310).

The trunk link frame location provided for the IR test in the IRL, as stored in the IR earlier, is passed to the AMRST through the MCA relay (SFD-L314).

Class indications passed from the register through the marker and master test frame connector are recorded in the AMRST through the make contacts of MCG and MCH relays. The detailed operation is explained in L3-2.5 CCK test.

The called number information passed from register to marker is closed through to the AMRST via its MCB relay. Five leads for each of eleven digits, and an M7 lead to register a 7 beyond the last digit are provided. Relays KA-L(2/5) operate in each digit position to correspond to the information passed from register to marker (SFD-L317). The operated relays lock and control the number checking path in combination with the register relays operated from keys or switches of the MTC circuit at the start of the test.

L3-2.4 RELEASE OF MARKER AND MASTER TEST FRAME CONNECTOR

The TRT tube and associated relays comprise a timing circuit which determines how long the marker will be held. Relay TRT1 operates through make contacts of MT, RPE2, and CI to start the timing (SFD-L320). Thus, timing is started as soon as both the CM and the MTFC have been seized. The TRT timing interval of 165 to 245 milliseconds is sufficient enough to permit operation of the cut-in relays at the marker and monitor ends of the master test frame connector and also the operation of the AMRST relays which record the information received from the marker.

Relay TRT1 closes the charging circuit for the TRT capacitor which charges in series with the TRT relay and the TRT3 resistor. When the TRT capacitor charges to approximately 70-volts, the TRT tube ionizes across its control gap 1 to 4. With the tube ionized, current flows in the main 1-2 gap to operate the TRT relay. The TRT operates the MKR relay which locks. Relay MKR connects ground to the DIS lead to the marker operating the DIS1,2 relays which operates the MRL relay of the register. This releases the marker connector and the marker.

If the MTFC is busy at the time the AMRST starts to select it, the monitor will wait until it becomes idle. The marker will be held during this period. If the master test frame connector is busy for a long interval, a 2.25-second timer in the marker will function to release the marker and sound an alarm. When the marker releases itself, MT will release and open the circuit to MKR. The trouble lamp will light, and the MST lamp will remain lighted as an indication that the marker phase of the call was not completed satisfactorily. If the register does not reach the marker, the test will end similarly but there will be no marker alarm.

In addition to releasing the CM and IR as just described, the MKR relay also operates the RTC1 relay (SFD-L117). Relay RTC1 locks and opens the TRST lead to release the monitor preference relay MON in the MTFC (SFD-L309). The MON then releases CI which removes ground from the ON lead to the MTFC to complete its release. Relay CI removes ground from the MKB lead to the marker to release the cut-in relays at the marker end of the master test frame connector if the release of the marker has not already progressed to the point of releasing these relays. Relay CI releases CII which releases MCA, MCB, MCG, MCH, and MCQ at the monitor end of the connection to the marker. When the MTFC completes its release, MTR1 is released. Relay RTC1 and MTR1 remove ground from the MON1 lead to the marker, but this action is not required for register testing since the marker is already releasing. Relay RTC1 also operates RTC2 which closes a path to the winding of the CKS relay.

L3-2.5 CCK TEST

Having called in a CM, the IR sends it an indication of the class of incoming trunk (SFD-L312). Facilities are provided to set up any possible trunk class in the register through the link. Early in the test, ground from a key or switch in the MTC circuit is connected over one of several leads, a make contact of the operated TCL relay, over a C lead to the IRL and thence to the register, where a class relay operates and locks (SFD-L113). The class relay helps to regulate the functions of the register and also grounds two or three leads to the marker to indicate what translator to use, the class of trunk, and whether a special marker is required to handle no test or similar features. These leads to the marker are brought back through the MTFC to contacts of cut-in relays MCG and MCH to the windings of translator and class recording relays in the AMRST (SFD-L312).

The AMRST is arranged to check that the IR has grounded the proper combination of class and translator leads to the marker on a 1-out-of-x basis. If the proper combination is not received, an immediate trouble record will be taken if the AMRST is arranged for checking interchangeable and NPA information codes. If the AMRST is not arranged for checking interchangeable and NPA information codes, it must timeout before indicating trouble. If the proper combination is received, then either relay CCK or NDK operates to indicate a satisfactory check.

An example of the matching circuit, where the test circuit is not arranged for checking interchangeable and NPA information codes (SFD-L113 option A and M), assume that the MTC circuit grounds lead OA. This operates the OA relay in the IR. When the IR seizes the CM, relay OA

grounds leads OA and INC, operating relays OA and INC in the AMRST (SFD-L312). The ground on lead OA from the MTC (SFD-L315 option A and M) then finds a path through a break contact of relay SPL, a make of OA, a break contact of OB and FVD, a make of INC, a break of key RRO, a break of relays RR3, PHC, THC, a break of keys RLR, DC, and BLR, a break of relay LR, key TST, and relay TST and IRPS, to the winding of class check relay CCK, which operates. A summary of class relay operations is shown in the following table:

Class and Translator Relay Operations Where the AMRST is not Arranged for Interchangeable and NPA Information Codes

<u>Lead Grounded By Control Circuit</u>	<u>Monitor Class Relays Operated</u>
OA	INC, OA TCA
OAS	INC, OA, SPL TCA
OB	INC, OB TCA
OBS	INC, OB, SPL TCA
AB	INC, FVD TCA
ABS	INC, FVD, SPL TCA

In order to make the class check, (when the test circuit is arranged for checking interchangeable and NPA information codes, option STD), the AMRST requires the presetting of the following three switches in the MTC circuit;

- (a) ICL, incoming trunk class switch
- (b) CL, class group switch
- (c) TRNC, translator lead switch C in addition to regular keys operated at the MTC circuit.

Ground for the check circuit is now through make contacts of IRST and MSTB, through the preset ICL switch, through a make contact of INC relay, through break of SPL key and relay, through the preset CL switch, through a make contact of one class group relay TAC or TCB, to the preset TRNA and TRNC switches, to a make contact of the OA relay, through a make contact of MSTB, break contacts of key RRO, break of TIR1, RLR, DC, and BLR, break contacts of relay LR, key TST and relay TST, break contacts of relay IRPS to the winding of class check relay CCK (SFD-L315).

If the LT and TT translator leads are combined in the CM, marker, the TRNA switch may be set for either the LT or TT translator lead check. A summary of class relay and translator relay operations is shown in the following table:

Class and Translator Relay Operations where the AMRST is Arranged for Interchangeable and NPA Information Codes

<u>Lead Grounded By Control Circuit</u>	<u>Monitor Class Relays Operated</u>	<u>Monitor Translator Relays Operated</u>
OA	INC, TCA	OA
OAS	INC, TCA	OA, SPL
OB	INC, TCA	OB
OBS	INC, TCA	OB, SPL
AB	INC, TCA	FVD
ABS	INC, TCA	FVD, SPL

L3-2.6 NUMBER CHECKING

If all the tests imposed on the IR are completed satisfactorily, a ground is connected to operate CKS through a contact of RTC2 (SFD-L323). The circuit details of the check path are covered in the descriptions of the individual tests in paragraphs which follow.

When CKS operates, it locks and lights the CKS progress lamp to indicate that the number is being checked.

The CKS also connects resistance battery to operate CKN if the numbers registered check (SFD-L324). When DIR2 or MIR2 operated from the start key of the MTC circuit, it operated the RTC relay which connected five leads for each code and digit key or switch of the master test control to the digit register relays (SFD-L116). For instance, the A0, A1, A2, A4, and A7 leads are connected respectively to the A0, A1, A2, A4, and A7 relay in the AMRST. The number set up on the key or switches, which was the number pulsed into the IR, operates the register relays on a 2-out-of-5 basis. Each of these relays is paired with a corresponding relay which records the number passed from register to marker. For instance A0, A1, A2, A4, and A7 are paired respectively with KA0, KA1, KA2, KA4, and KA7 (SFD-L324). The check path is wired through the make contacts of the pair in series. Hence, completion of the check path requires that the two numbers be exactly the same. At the time CKS closed battery to the check path, it also closed the operating path for CKE (SFD-L325). Relay CKE is slow-operate to permit the CKN to operate if the check path is complete. When CKE operates, ground is connected through break contacts of CKN to operate TRR1 and cause a trouble record to be made, or through make contacts of CKN to operate OK.

L3-2.7 TROUBLE RECORD (SFD-L325)

When TRR1 operates, it locks and operates TRR2. Relay TRR2 opens the OK operating path to prevent a late number check from operating the OK relay. The MKB lead is opened by TRR1 to prevent operating marker cut-in relays.

Relay TRR1 closes battery to the TRST lead to operate the monitor preference relay MON in the master test frame connector (SFD-L309). When the AMRST gains access to the MTFC, CI operates. Relay CI closes ground to the ON lead to operate off-normal relays in the master test frame connector and another ground from break contacts of TRR1 to the STR lead. The STR lead ground is extended through the MTFC to the trouble recorder control circuit which prepares the trouble recorder and master test frame connector to receive a trouble record. The CI also operates the CII relay which operates MCA, MCB, MCD, MCE, MCG, and MCH relays.

The primary objective of this trouble record is to utilize the facilities of the trouble card to indicate the pulsing performance of the register. The KAL(2/5) relays previously operated to record the called number passed from register to marker extend their locking grounds into the master test frame connector through the MCB relay (SFD-L316). Similarly the called number registered by the AMRST from the MTC circuit is extended through the MCE relay to the MTFC (SFD-L116). The MCG and McGaud MCH relays are used to obtain the classes previously recorded (SFD-L312).

Additional information is also included in the trouble record. The MIR lead to the master test frame connector is grounded through DIRI or MIR1 and MCA to indicate that the trouble record is being made by the AMRST on an IR call (SFD-L326). The SRT lead through STT and MCA indicates that it is a test call. The CM number is recorded through the MCA relay (SFD-L310). Relay MCA connects ground to the RG, CN, and FR leads to the IR where they are extended through the M relay to leads to the MTFC which identify the register (SFD-L326). The RG, FR, and CN leads are used respectively to indicate the position of the register in its marker connector, the frame on which the marker connector is located, and the position of the marker connector on that frame. The information recorded through the MCD relay is also included in the trouble record. This information indicates register response to certain tests imposed on it.

After a trouble card has been perforated in accordance with information conveyed by grounded leads extending from the AMRST to the trouble recorder through the MTFC, ground is connected to the TRC lead to operate the TRC relay which locks (SFD-L326). Relay TRC opens the TRST lead to release the master test frame connector, trouble recorder, and the CI, CII, MCA, MCB, MCD, MCE, MCG, MCH, and MTR1 relays of the AMRST. Relay TRC also operates TBL.

L3-2.8 TEST COMPLETION

When CKN operates as an indication that the number check is satisfactorily completed, and when TAC2 operates as a sign that the IR has started its release, the OK relay operates, and locks under control of TAC2 (SFD-L325). Relay OK lights the OK lamp and extinguishes the CKS lamp. The OK operates the TA relay to stop timing of the test and also opens the operating circuit of TBL (SFD-L326).

When an abandoned call test is made, if the IR releases satisfactorily, TAC2 will operate and close a ground to operate the OK relay. If the IR fails to release and selects the marker, the operating path for OK just described will be opened at RPE2 and the test will fail because the operating path for CKS will be open.

If the IR fails to perform satisfactorily during the tests, the TBL relay will operate (SFD-L326). Relay TBL locks and lights the TBL lamp. Relay TBL opens an operating path of the CKS relay to prevent the start of a number check. Relay TBL opens the operating path of the OK relay and also operates TA to stop timing of the test.

Relay TBL may operate as a result of a number check failure, in which case it operates from TRC as described previously. In certain tests a positive indication of trouble is obtained, and TBL is operated directly. In other cases, the only indication of trouble will be that the operate path of the CKS relay will be open. Under this condition the TM timer will function to operate the TBL relay.

During the waiting period required for class check, the CTT relay operates (SFD-323). Relay CTT lights the CCK progress lamp, connects ground through RTC2 to a contact of TM1, and opens the normal operating path of TBL. If the class check fails, TM1 will operate as a result of a timeout and will operate TRR1 to cause a trouble record to be made as covered earlier. If the test employee does not wish to wait 40 to 70 seconds for a timeout, operating the QTR key, after the CCK progress lamp lights but before CKS lamp lights following marker release, will cause an immediate trouble record. Since this trouble record shows the class information passed from register to marker and recorded in the AMRST through the MCG and MCH relays, it may be desirable to obtain the trouble record even though there is no class check failure. In this case, operation of the QTR key, before CKS lamp lights following marker release, will cause a trouble record immediately after CTT operates.

When the OK relay operates, it removes the 10-ohm ground from the TAC relay. This permits the ON relay of the IR to release and start complete release of the register. The M, MB, and RB relays of the register will, however, be held operated until the AMRST is released. If the TBL relay operates, the ON relay of the IR will not be released, thus permitting inspection of the register while in its off-normal condition.

L3-2.9 RELEASE

The operation of the RL key of the MTC circuit operates the KR relay which removes ground from the STG lead releasing the BT2 relay (SFD-L109). The BT2 releases IRP relay which releases the register M relay which permits complete release of the register. Relay IRP also releases DIR2 or MIR2 which causes the release of relays which function on every call. When BT2 releases, BT1 operates and, when TSR releases, battery is closed to the N lead to the MTC circuit to permit another call to be started. Relay TSR is slow-release to permit all relays of the AMRST to release before permitting reseizure.

L3-2.10 REPEAT TEST

Operation of the REP key of the MTC circuit causes repeat tests to be made. The call progresses as previously described for an OK call up through the point of operating the OK relay. The OK relay closes ground to the REP lead to the master test control circuit to shunt down its Ni relay which removes ground from the STG lead to release the AMRST. When TSR releases and closes battery to the N lead, the MTC circuit proceeds to initiate another test call. If a trouble is encountered, TBL will operate to sound an alarm from battery received on the AL lead from the REP key of the master test control circuit, and no further tests are made.

L3-2.11 LR AND DC TESTS

The incoming registers are arranged to time the link functions of connecting a trunk to an IR and to report trouble if the link relays are not released within a reasonable time. In addition, the registers check for double connections in the line switches and, if they find one, time out and report the trouble. These features are tested by operating link release key RLR or double connection DC respectively. Any trunk class may be used; digit keys or switches are required only for bylink tests of these features. Key RLR opens the operating circuit for relay NDT preventing registration of trunk class in the register (option A and M), or the TCL switch at the master test control circuit is set to the off position to prevent the registration of trunk class in the IR (STD option). The DC key holds a direct ground on lead HM, simulating a double connection. Either RLR or DC key operate "special feature test" relay SFT.

The test is started in the usual manner and proceeds through tests RB, LO, LK, OH, and CO as on a normal test. Next, the register RLK relay would normally operate to release the link, but, due to key RLR or DC being operated, the register should detect the lack of trunk class information or the simulated double connection and block. The register

link release timer LR should function and call in a CM, indicating the timeout by grounding lead LR and, on double connection tests, indicating the nature of the trouble by withholding ground from lead DCK. When the AMRST is connected to the marker, LR operates (SFD-L313), locks, and operates TM2 to shorten the test timing (SFD-L125). The marker then sends the register a trouble release signal, causing the IR to remove battery from lead LK. This releases the LK relay (SFD-L112) of the AMRST and the link as described under RLK test. The release of relay LK advances the progress indication from lamp RLK to contacts of relay D, the WS and WL lamps being bypassed by operated contacts of relay SFT. Relay D should have been operated from ground on the D lead in the register when the register called for a marker. Relay NDK operates on a circuit from battery through its winding, make contact of relay LR, and either make of relay DCK and key RLR to ground or break of relay DCK and make of key DC to ground (SFD-L315). Relay NDK connects ground from the progress indication lead to operate OK as an indication that the test is satisfactory and that the digit timing test and digit check should be omitted (SFD-L325).

The withholding of class information from the IR on the LR test is done by opening the operating circuit of the NDT relay or by setting the TCL switch at the master test control circuit to the off position. In offices where they are not equipped and certain contacts are looped so that the class information cannot be withheld in this manner the LR test should not be made. The LR lead from the register to the marker will be checked on the DC test, and DCK lead from the register to the marker will be checked on a regular service call.

If the IR does not remove battery from the LK lead, the AMRST will timeout and operate TBL to light the TBL lamp. Relay TBL also operates LKT which will release the link. Failure of the LR or DCK relays to operate when they should during the test will cause a timeout trouble record by leaving NDK unoperated and operating CTT but not CCK. Under this latter condition, the RBT relay is operated through the RLR or DC key to insure a trouble release of the register.

No digits are sent on LR or DC test by direct pulsing or MF, because relays DLP and MFP have no operating circuits.

L3-2.12 ABANDONED CALL TEST

This test checks the operation of incoming registers on early abandoned calls. With MF registers, it makes a release current flow test on the register supervisory relay.

When making this test, key RAB should be operated, which operates incoming register abandoned relay IRAB (SFD-L208). Any trunk class key may be operated but no digit keys or switches are needed. The test is started in the usual manner and proceeds through tests RB, LO, LK, OH, CO, WS, and WL as on a normal call. When all of these tests have been completed, the register supervisory relay is released because the loop is opened at contacts of relay IRAB. The supervisory relay L of the DP register is normally held after the wink over leads T and R, through make-contacts of relays NBL and C, a make of DLP and a break of IRAB (SFD-L224). Since the IRAB relay opens this path, the register should recognize an abandoned call as soon as it looks at its supervisory relay. The supervisory relay of MF registers is normally held over lead R through make-contacts of relays NBL and C, break contacts of relays DLP1 and IRPS, break of IRAB, windings of TG, break contacts of DLP1, make contacts of C and NBL to lead T (SFD-L228). The MF pulses are superimposed on this circuit from the MF generator. On MF tests, IRAB opens the circuit to the TG relay and the register supervisory relay A must release against the A resistance which is connected across the T and R leads through make contacts of relays IRAB and WOK. When the register supervisory relay releases, the register should release immediately without calling in a marker. Satisfactory completion of this test is indicated by operating OK through a make contact of relay IRAB to the progress indicating ground (SFD-L325). Should the IR call for a CM erroneously, the operate path of the OK is opened by the operation of relay RPE2.

L3-2.13 PERMANENT SIGNAL TEST

This test checks the operation of the IR on calls on which pulsing of digits is expected but does not occur. With the MF register, it also makes an operate current flow test on the register supervisory relay.

When making this test, keys RRO and RPS should be operated, the latter operating incoming register permanent signal relay IRPS (SFD-L208). Any trunk class key may be operated, but no digit keys or switches are needed. Relay IRPS operates relay SFT, which cancels the wink test. Testing is started in the usual manner and proceeds through tests RB, LO, LK, OH, CO, and LK as on a normal call. When all of these tests have been completed, the register supervisory relay should remain operated, and the IR should time out. Dial and MF pulsing do not occur because the start pulsing leads are opened at contacts of relay IRPS. The MF register supervisory relay must operate in series with the A0 resistor which is connected across the T and R leads through a make contact of relay IRPS. This constitutes an operate current flow test relay. On direct dial pulse permanent signal tests, the A0 resistor is shorted, no attempt is made to test the register supervisory relay on a current flow basis because it is tested adequately by pulsing.

When the IR times out, it operates the D relay and calls in a CM, withholding trunk class information and grounding lead R0. The AMRST should then make its CCK test, operating relay NDK on a circuit from its winding through a make contact of relay IRPS (SFD-L315). Relay NDK indicates satisfactory completion of the test by operating OK.

L3-2.14 REORDER TESTS

When any test is made which would result in ground on the R0 lead to operate the R0 relay in the AMRST, key RRO should be operated. This arranges the CCK test so that relay R0 must operate to check out (SFD-L315). Failure of R0 to operate will cause a trouble record to be made which includes the class indications passed from IR to CM. One example of an R0 test is the incoming register permanent signal test described above.

L3-3 SENDER (SDR) TEST

After the OS completes outpulsing, the digits outpulsed by the sender into the AMRST are checked against the digits that were stored in the monitor at the start of the test by the MTC. If the digits match, the test has been completed satisfactorily and an OK signal is indicated. This starts release of the OS. Operation of the RL key in the MTC starts release of the AMRST, however, the AMRST and sender will not fully release until the STT key in the AMRST has been released.

L3-3.1 PULSE END AND NUMBER CHECK

Where the tests imposed on the OS permit it to complete pulsing, the sender will ground the SPE lead to the AMRST. This ground will operate the SPE relay (SFD-L240). When trunk closure has been checked, as indicated by TCT operating, SPE1 will operate. Relay SPE1 closes ground to operate PE when PH releases on DP senders. Relay PE connects ground through break contacts of the AS relay and make contacts of an operated steering relay and operates the -7 register relay of the digit one beyond the last pulsed digit (SFD-L236). Relay PE is made slow-operate and its operating circuit wired through break contacts of PH to insure that the monitor steering circuit advances to the next position before a -7 relay is operated. The PE also operates CKS (SFD-L322) which is slow-operate to permit the -7 relay to operate before the check is started. Relay CKS closes resistance battery through the number check path. If the numbers registered check, this battery is returned to operate CKN.

Each relay used in registering the outpulsed number as received by the AMRST is paired with a corresponding relay which records the number passed from MTC circuit to CM. For instance, A0, A1, A2, A4, and A7 (SFD-L236,7) are paired respectively with KA0, KA1, KA2, KA4, and KA7 (SFD-L122).

The check path is wired through the break contacts of a relay pair in series, a paralleling path being wired through the make contacts of the pair in series. Hence, completion of the check path requires that the two numbers be exactly the same for CKN to operate (SFD-L324).

At the time CKS closed battery to the CKN path, it also closed the operating path for CKE (SFD-L325). Relay CKE is slow-operate to permit CKN to operate if the check path is complete. When CKE operates, ground is connected through break contacts of CKN to operate TRR1 and cause a trouble record to be made, or through make contacts of CKN to operate OK.

L3-3.2 TROUBLE RECORD

When TRR1 operates, it locks and operates TRR2 (SFD-L325). Relay TRR2 opens the OK operate path to prevent a late number check from operating the OK relay. Relay TRR1 closes resistance battery to the TRST lead to operate the monitor preference relay MON in the MTFC (SFD-L309). When the AMRST gains access to the MTFC, CI operates. Relay CI closes ground to the ON lead to operate off-normal relay ON in the master test frame connector and another ground from make contacts of TRR1 to the STR lead. The STR lead ground is extended through the master test frame connector to the trouble recorder control circuit which prepares the trouble recorder and MTFC to receive a trouble record. Relay CI also operates the CII relay which operates MCA, MCB, MCC, MCE, MCI, and MCQ.

The primary objective of this trouble record is to utilize the facilities of the trouble card to indicate the pulsing performance of the OS. The KA-L(2/5) relays, previously operated to record the number passed from the master test control circuit to the marker, extend their locking grounds into the master test frame connector through the MCB relay (SFD-L122). The outputted number registered by the AMRST is similarly extended through the MCE relay (SFD-L236,37).

The OTL location (SFD-L120) and the marker number are recorded through the MCA relay (SFD-L310). The location of the outgoing trunk is recorded through the MCC relay (SFD-L118). The MOS lead to the master test frame connector is grounded through the MCI to indicate that the trouble record is being made by the AMRST on an OS call (SFD-L326). The SRT lead is grounded through STT and MCA to indicate that it is a test call. Relay TR and TR2 operate when a trouble record is made and furnish ground for indicating the information relative to the outputted number passed from marker to sender and recorded in the AMRST through the MCI and MCJ relays.

Relay MCA connects ground to the S, CN, and FR leads to the OS where they are extended through the M relay to leads to the master test frame connector which identify the sender. The S, FR, and CN leads are used to indicate the position of the sender in its OSC, the frame on which the connector is located, and the position or the OSC on that frame, respectively (SFD-L326).

After a trouble card has been perforated in accordance with information conveyed by grounded leads extending from the AMRST to the trouble recorder through the MTFC, a ground is connected to the TRC lead of the MTFC to operate the TRC relay (SFD-L326). Relay TRC locks and opens the TRST lead to release the master test frame connector, trouble recorder, and the CI, CIl, MCA, MCB, MCC, MCE, MCI, MCJ, and MTR1 relays, of the AMRST. Relay TRC also operates TBL.

Under certain conditions, a trouble record card is obtained under control of the MTC circuit to obtain the information transmitted by the CM to the OS. This may delay the operation of the sender AV relay until after the normal functioning time of the TMX and TMX1 timers. To prevent false trouble conditions, the REC1 and REC2 relays are operated to stop these timers while such records are being made.

L3-3.3 TEST COMPLETION (SFD-L325)

When CKN operates as an indication that the number check was satisfactorily completed, it connects ground to make contacts of TAC2. When TAC2 operates to indicate that the sender has started to release, this ground operates the OK relay which locks under control of TAC2. Relay OK lights the OK lamp and extinguishes the CKS lamp. Relay OK operates the TA relay to stop timing of the test and opens the operating circuit of TBL.

If the OS fails on any of the tests, the TBL relay will be operated to light the TBL lamp (SFD-L326). Relay TBL operates the TA relay to stop the timing and opens the operating path of relay OK. Relay TBL may operate from TB1 or TB2 as a result of a sender test failure, or as a result of a number check failure in which case TBL operates from TRC as described previously. In case the test is not completed within the TM timer interval, TBL operates from TM1.

When the OK relay operates, it removes the 10-ohm ground from the winding of the TAC relay (SFD-L208). This permits the ON relay of the OS to release and start the complete release of the sender. The M and SB relays of the sender will, however, be held operated until the AMRST is released. If TBL operates, the ON relay of the sender will not release, thus permitting inspection of the OS while in its off-normal condition.

L3-3.4 RELEASE

The operation of the RL key of the MTC circuit operates the KR relay which removes ground from the STG lead releasing the MOS2 or DOS2 relay which releases ONT1 and ONT2 and opens all leads to the sender permitting its release. Release of these relays cause the release of all operated relays associated with the particular call. Relay TSR releasing from ONT1 recloses battery to the N lead to the MTC circuit to permit another call to be started. Relay TSR is slow-release to permit all relays of the AMRST to release before permitting reseizure. To completely release the AMRST, the STT key should be restored to normal.

L3-3.5 REPEAT TESTS

Operation of the REP key of the MTC circuit causes repeat tests to be made. The call progresses as previously described for an OK call up through the point of operating the OK relay. The OK relay closes ground to the REP lead to the MTC circuit to shunt down its N1 relay which removes ground from the STG lead to release the AMRST. When TSR releases and closes battery to the N lead, the master test control circuit proceeds to initiate another test call. If a trouble is encountered, TBL will operate to sound an alarm from battery received on the AL lead from the REP key of the master test control circuit.

L3-3.6 MARKER TROUBLE RELEASE

If the CM encounters trouble in setting up the connection or attempts to disconnect before operating the hold magnets, it will operate MTR (SFD-L326). Relay MTR locks and releases C11 which releases the MCA, MCB, MCC, MCI, and MCJ relays. Relay MTR operates NRR which removes ground from the MON1 lead to release the MON1 relay of the marker. Release of the MON1 relay permits the marker to make a trouble record and release. Under this condition, the AMRST will time out and operate the TBL relay.

